CH32V208 Datasheet

V2.6

Overview

The CH32V series is an industrial-grade general-purpose microcontroller based on the 32-bit RISC-V design of Qingke.

Designs such as fast interrupt entry greatly improve the interrupt response speed compared with the standard. CH32V208 is equipped with V4C core and adds memory protection function. Reduce hardware division cycles. Product functions support 144MHz main frequency zero-wait operation, and this series of products integrates 2Mbps low-power Bluetooth BLE communication module, 10M Ethernet MAC+PHY module, USB2.0 full-speed device+host/device interface, CAN controller, etc.

Product Features

l Core:
- Qingdao 32-bit RISC-V core, multiple instruction set combinations
- Fast programmable interrupt controller + hardware interrupt stack
- Branch prediction and conflict handling mechanism
- Single cycle multiplication, hardware division
- System clocked at 144MHz

l Memory:
- Can be configured with a maximum of 64KB volatile data storage area SRAM - Can be configured with 480KB program storage area CodeFlash (zero wait application area + non-zero wait data area)
- 28KB system boot program storage area BootLoader - 128B system non-volatile configuration information storage area
- 128B user-defined information storage area

l Power management and low power consumption: - System power supply VDD rated: 3.3V - GPIO unit independent power supply VIO rated: 3.3V - Low power consumption mode: sleep, stop, standby
- VBAT power supply independently powers RTC and backup registers

l System clock, reset
- Built-in factory-trimmed 8MHz RC oscillator
- Built-in 40KHz RC oscillator
- Built-in PLL, optional CPU clock up to 144MHz - External support for 32MHz high-speed oscillator
- External support 32.768KHz low-speed oscillator
- Power-up/power-down reset, programmable voltage monitor

l Real-time clock RTC: 32-bit independent timer l 1 set of 8-way general-purpose DMA controller
- 8 channels, support ring buffer management
- Support TIMx/ADC/USART/I2C/SPI

l 2 sets of operational amplifiers and comparators: connected to ADC and TIMx l 1 set of 12-bit analog-to-digital conversion ADC
- -Analog input range: VSSAÿVDDA - 16 external signals + 2 internal signal channels
- On-chip temperature sensor
- Dual ADC conversion mode

l 16 TouchKey channel detection l Multiple sets of timers
- 1 16-bit advanced timer with dead-band control and emergency Brake, providing PWM complementary output for motor control
- 3 16-bit general-purpose timers providing input capture/output ratio Comparison/PWM/pulse counting and incremental encoder input
- 1 x 32-bit general-purpose timer
- 2 watchdog timers (independent and windowed)
- System time base timer: 64-bit counter

l Multiple communication interfaces:
- 4 USART interfaces
- 2 I2C interfaces (support SMBus/PMBus)
- 2 SPI interfaces
- USB2.0 full-speed device interface (full speed and low speed)
- USB2.0 full-speed host/device interface
- 1 CAN interface (2.0B active)
- Built-in 10M PHY transceiver
- Bluetooth Low Energy BLE5.3 l Fast GPIO Ports - 53 I/O ports, mapped to 16 external interrupts

l Security features: CRC calculation unit, 96-bit chip unique ID l Debug mode: Serial 2-wire debug interface l Package: LQFP and QFN

Chapter 1 Product Description

The CH32V series products are industrial-grade general-purpose enhanced MCUs designed based on the 32-bit RISC-V instruction set and architecture. Resources are divided into general, connection, wireless and other categories. They are divided into packaging categories, peripheral resources and quantity, number of pins, device characteristics, etc. The differences in height extend to each other, but they remain compatible with each other in terms of software, functions, and hardware pin configuration, providing users with a better understanding of the product development process. Product iteration and rapid application provide freedom and convenience.

Please refer to the data sheet for device characteristics of this series of products.

For detailed information on the product peripheral function description, usage methods, register configuration, etc., please refer to "CH32FV2x_V3xRM".

Both the data sheet and reference manual can be downloaded from Qinheng's official website: www.wch.cn. Related information about the RISC-V instruction set and architecture can be downloaded from the "http://riscv.org" website.

This manual is the data sheet for the CH32V208 series products. For the V203 series, please refer to "CH32V203DS0", for the V303_305_307 series, please refer to Refer to "CH32V307DS0".

Table 1-1 Product series overview

Small and medium capacity general purpose		Large-capacity universal type (V303)		Connected type (V305)	Interconnected type (V307)	Wireless type (V208)
(V203) Highland barley V4B		Highland Barley V4F				Highland Barley V4C
32K Flash 64K Flash 128K Flash 256K Flash		128K Flash	256K Flash	128K Flash		
10K SRAM	20K FOR SHAME	32K SRAM	64K SRAM	32K SRAM	64K SRAM	64K SRAM
2*ADC(TKey) ADTM 3*GPTM 2*USART SPI 2C USBD USBFS CAN RTC 2*WDG 2*OPA	2*ADC(TKey) ADTM 3*GPTM 4*USART 2*SPI 2*I2C USBD USBFS CAN RTC 2*WDG 2*OPA	2*ADC(TKey) 2*DAC ADTM 3*GPTM 3*USART 2*SPI 2*I2C USBFS CAN RTC 2*WDG 4*OPA	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 8*USART/UART 3*SPI(2*I2S) 2*I2C USBFS CAN RTC 2*WDG 4*OPA RNG SDIO FSMC	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 5*USART/UART 3*SPI(2*I2S) 2*I2C OTG_FS USBHS(+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 8*USART/UART 3*SPI(2*I2S) 2*I2C OTG_FS USBHS(+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO FSMC PAD ETH-1000MAC 10M-PHY	ADC(TKey) ADTM 3*GPTM GPTM(32) 4*USART/UART 2*SPI 2*I2C USBD USBFS CAN RTC 2*WDG 2*OPA ETH-10M(+PHY) BLE5.3

Note: The number or functions of some peripherals in the same category may be limited by the package. Please confirm the product package when selecting.

abbreviation

ADTM: Advanced Timer

GPTM: General purpose timer

GPTM(32): 32-bit general purpose timer

BCTM: basic timer

TKey: Touch key

OPA: operational amplifier, comparator

RNG: random number generator

USBD: Full-Speed Device Controller

USBFS: Full-Speed Host/Device Controller

USBHS: High Speed Host/Device Controller

Table 1-2 Kernel comparison overview

Features / Kernel	Instruction Set	hardware Stack series	interrupt Nested series	fast Interrupt Number of channels	integer division cycle	vector table model	Extensions instruction	Memory Protect
V4B	IMAC	2	2	4	9	Address or instruction support	None	
V4C	IMAC	2	2	4	5	Address or command support	standard	
V4F	IMAFC	3	8	4	5	Address or command support	standard	

Note: For relevant information about the kernel, please refer to the QingKeV4 microprocessor manual "QingKeV4_Processor_Manual".

Chapter 2 Specifications

The CH32V208 series is a 32-bit RISC core MCU designed based on the RISC-V instruction architecture, with an operating frequency of 144MHz and built-in high-speed storage. The system architecture has multiple buses working synchronously, providing rich peripheral functions and enhanced I/O ports. It also includes functions such as ADC module, multiple timers, multi-channel touch button capacitance detection (TKey), and standard and dedicated communication interfaces: I2C, SPI, USART, CAN controller, USB2.0 full-speed host/device controller, USB2.0 full-speed device controller, Bluetooth low energy, etc.

The product has a rated operating voltage of 3.3V and an operating temperature range of -40ÿÿ85ÿ industrial grade. It supports a variety of power-saving working modes to meet the needs of production product low power application requirements. Each model in the series of products differs in terms of resource allocation, number of peripherals, peripheral functions, etc. You can choose according to your needs.

2.1 Model comparison

Table 2-1 Wireless product resource allocation

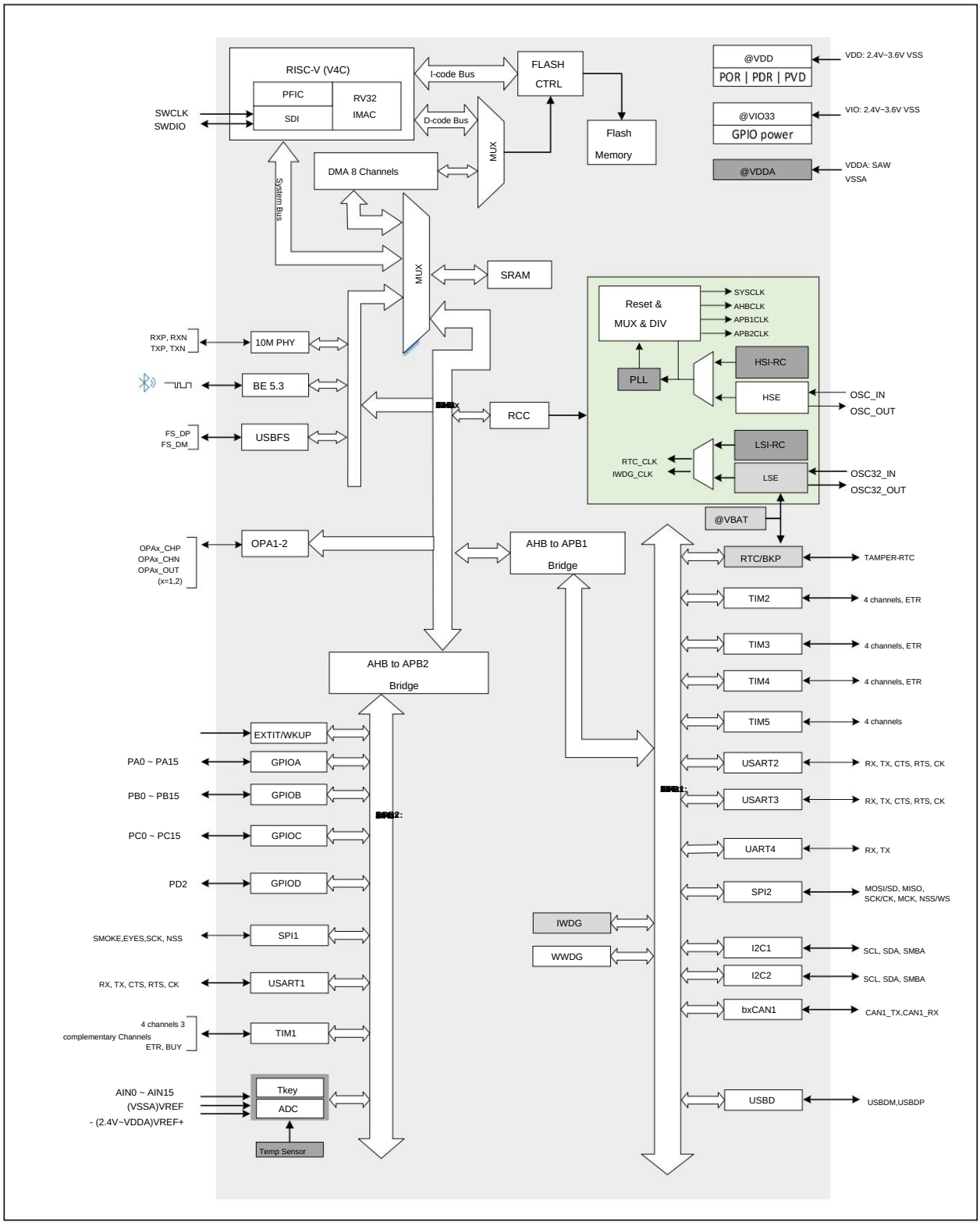
Product number / Resource differences			CH32V208			
			GB	CB	RB	WB
Number of chip pins			28	48	64	68
Flash memory (bytes) (1)			128K(2)	128K(2)	128K(2)	128K(2)
SRAM (bytes)			64K(2)	64K(2)	64K(2)	64K(2)
Number of GPIO ports			21	37	49	53
GPIO Power Supply			Shared with VDD			Independent VIO
Certainly hour Device	Advanced (16-bit) General		1	1	1	1
	(16-bit) General (32-bit)		3	3	3	3
	Watchdog System		1	1	1	1
	Timebase (24-bit)		2	2	2	2
RTC			support			
ADC/TKey (number of channels/unit) operational			8@1	16@1	16@1	16@1
amplifier, comparator			OPA2	2	2	2
Pass letter catch mouth	USART/UART		2	4	4	4
	SPI		1	2	2	2
	2C		1	2	2	2
	CAN		1	1	1	1
	USB(FS)	USBD	1	1	1	1
		USBHD	1	1	1	1
	Ethernet		10M		10M	
	BE 5.3		support			
CPU main frequency Rated			Maxÿ144MHz			
voltage Operating			3.3V			
temperature Package type			Industrial grade: -40ÿÿ85ÿ			
			QFN28	QFN48	LQFP64M	QFN68

Note: 1. The flash memory byte represents the zero wait operation area R0WAIT. V208 the size is 480K- R0WAIT FLASH+64K SRAM), (144K 2.128K Products with non-zero wait area support user-selected word configurations as (128K FLASH+64K SRAM 208 FLASH+48K SRAM), (160K FLASH+32K SRAM) one of several combinations.

2.2 System Architecture

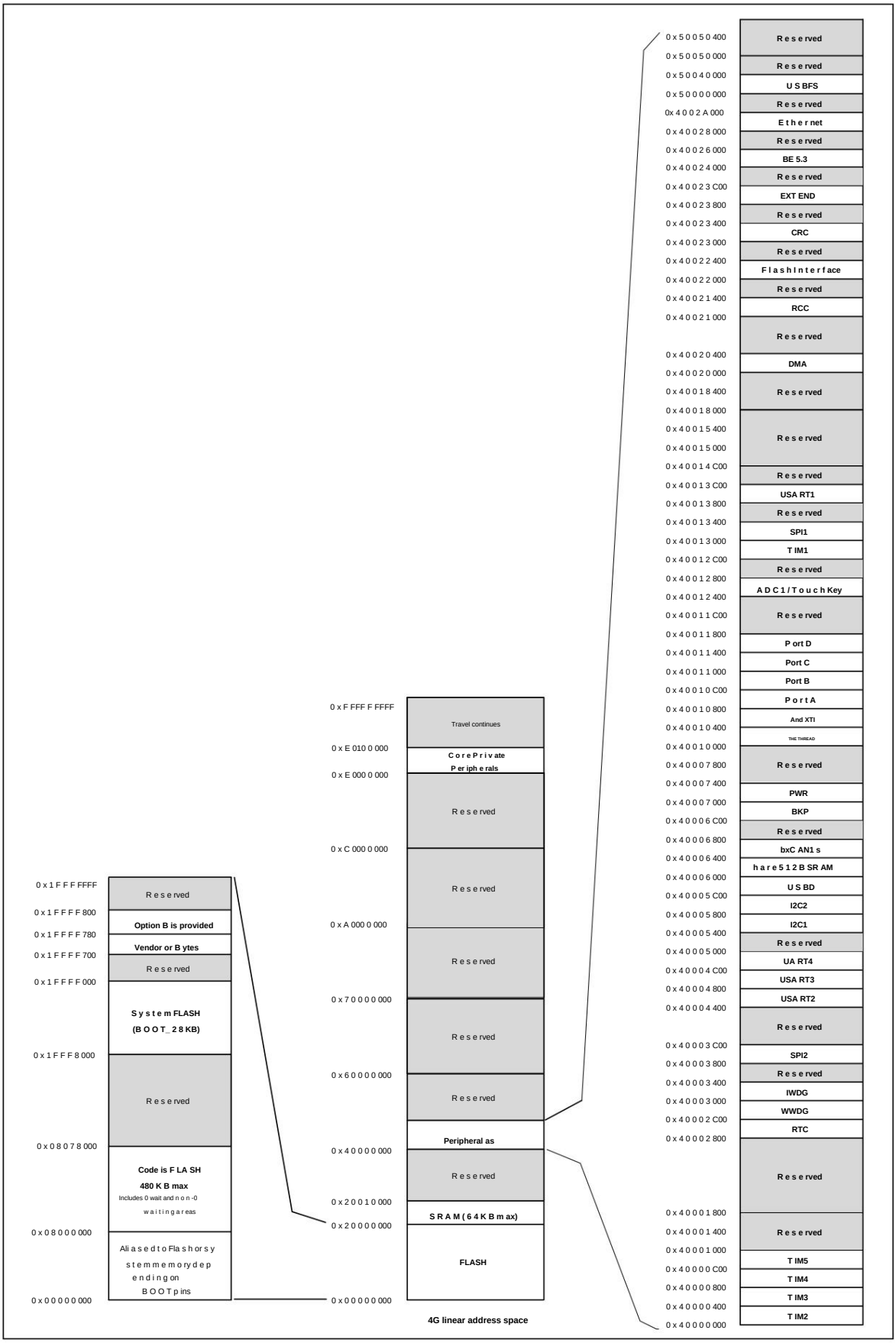
The microcontroller is designed based on the RISC-V instruction set. In its architecture, the core, arbitration unit, DMA module, SRAM storage and other parts interact through multiple sets of buses. The design integrates a general DMA controller to reduce the burden on the CPU and improve access efficiency. It applies a multi-level clock management mechanism to reduce the operating power consumption of peripherals. It also has a data protection mechanism, automatic clock switching protection and other measures to increase system stability. The figure below is a block diagram of the overall internal architecture of the series of products.

Figure 2-1 System block diagram



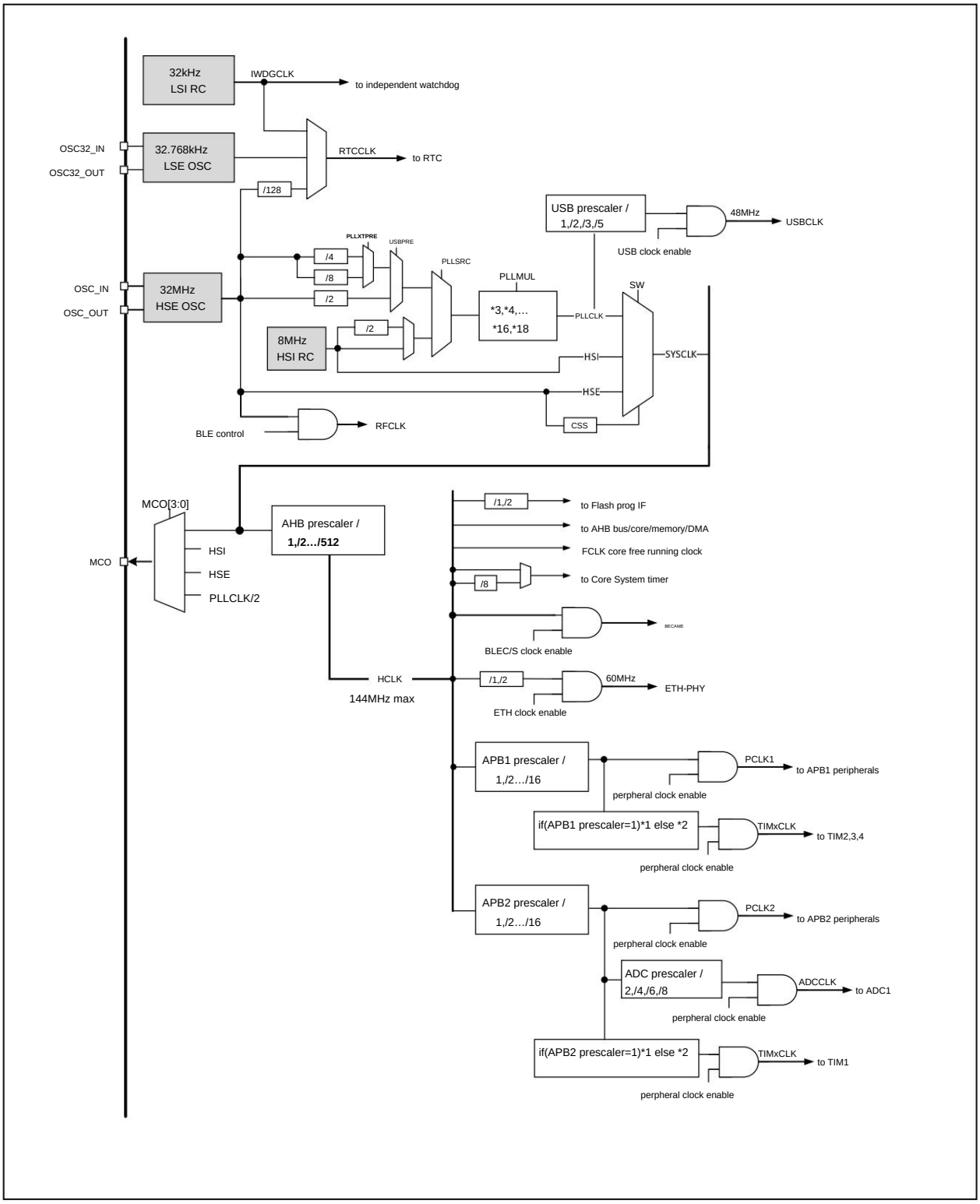
2.3 Memory Mapping Table

Figure 2-2 Memory address mapping



2.4 Clock Tree

Four groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly multiplied by PLL and output as the system bus clock (SYSCLK). The system clock is then provided by various pre-dividers to the AHB domain, APB1 domain, APB2 domain peripheral control clock and sampling or interface output clock. Some modules need to be directly provided by the PLL clock. Figure 2-3 Clock tree block diagram



Note: 1. When using this function, the CPU frequency must be 48MHz or 144MHz. USB 96MHz

When waking up, the system will automatically switch to the main frequency. If you use the said function at the same time, you need to select USBPRE=5DIV, and HSI USB ETH is configured as frequency PLLCKP=SYSCLK

240M, AHBPRE=2DIV, CPU 120M.

2. The external crystal or clock (HSE) of CH32V208 product is 32M. When using external crystal, no load capacitor is required and it is built-in.

2.5 Function overview

2.5.1 RISC-V4C Processor

RISC-V4C supports the IMAC subset of the RISC-V instruction set. The processor is managed in a modular manner, including units such as the fast programmable interrupt controller (PFIC), memory protection, branch prediction mode, and extended instruction support. Multiple external buses are connected to external unit modules to achieve interaction between external functional modules and the core. The processor can be flexibly applied to microcontrollers in different scenarios with its minimalist instruction set, multiple working modes, and modular Design, such as small-area low-power embedded scenarios, high-performance application operating system scenarios, etc. l Supports machine and user privilege modes l Fast programmable interrupt controller (PFIC) l Multi-level hardware interrupt stack l Serial 2-wire debugging interface l Standard memory protection design l Static or dynamic branch prediction, efficient jump, conflict detection mechanism l Custom extension directive

2.5.2 On-chip memory and boot mode

Built-in maximum 64K bytes SRAM area for storing data, which will be lost after power failure. The specific capacity should correspond to the chip model. Built-in maximum 480K bytes program flash storage area (Code FLASH) for user application and constant data storage. It includes zero wait program running area and non-zero wait area. The specific size of the area corresponds to the chip model.

Built-in 28K bytes of system storage area (System FLASH) for system boot program storage (factory fixed bootloader). 128 bytes for system non-volatile configuration information storage area, 128 bytes for user selected word storage area. At startup, one of three boot modes can be selected through the boot pins (BOOT0 and BOOT1): l Boot from program flash memory l Boot from system memory l Boot from internal SRAM The bootloader is stored in the system storage area, and the contents of the program flash storage area can be reprogrammed through USART1 and USB interface.

2.5.3 Power Supply Solution

l VDD = 2.4ÿ3.6V: Powers some I/O pins and internal voltage regulator. l VIO = 2.4ÿ3.6V: Powers most I/O pins and Ethernet module, and determines the pin output high voltage amplitude. Normal During operation, the VIO voltage cannot be higher than the VDD voltage.

l VDDA = 2.4ÿ3.6V: Powers the analog parts of high-frequency RC oscillator, ADC, temperature sensor, DAC and PLL. The VDDA voltage must be the same as the VIO voltage (if VDD is powered off and VIO is powered, VDDA must be powered and consistent with VIO). When using the ADC, VDDA must not be less than 2.4V.

l VBAT = 1.8~3.6V: When VDD is turned off, (through the internal power switch) the RTC, external low-frequency oscillator and rear Power supply for the backup register. (Note the VBAT power supply)

2.5.4 Power supply monitor This

product integrates a power-on reset (POR)/power-down reset (PDR) circuit. This circuit is always in working state to ensure that the system works when the power supply exceeds 2.4V; when VDD is lower than the set value threshold (VPOR/PDR), the device is placed in the reset state without using an external reset circuit. In addition, the system is equipped with a programmable voltage monitor (PVD), which needs to be turned on through software to compare the voltage of the VDD power supply with the set threshold VPVD. Turn on the corresponding edge interrupt of PVD, and you can receive an interrupt notification when VDD drops to the PVD threshold or rises to the PVD threshold. Refer to Chapter 4 for the values of VPOR/PDR and VPVD.

2.5.5 After the voltage regulator

is reset, the regulator automatically turns on. There are three operating modes according to

the application. l On mode: normal operation, providing stable core power supply l Low

power mode: when the CPU enters stop mode, you can select The regulator operates with low power

consumption. Shutdown mode: When the CPU enters standby mode, the regulator automatically switches to this mode. The output of the voltage regulator is in a high-impedanc

The power supply to the circuit is cut off and the voltage regulator is in a zero consumption state.

The voltage regulator is always in the on mode after reset, and is turned off in the shutdown mode in standby mode. At this time, it is a high-impedance output.

2.5.6 Low Power Mode The

system supports three low power modes, which can be selected to achieve the best balance between low power consumption, short startup time and multiple

wake-up events. l

Sleep mode In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low power mode, but can achieve the

fastest wake-up. Exit condition: any interrupt or

wake-up event. l Stop

mode In this mode, FLASH enters low power mode, and PLL, HSI RC oscillator and HSE crystal oscillator are turned off. While maintaining SRAM and Stop mode can achieve the lowest power consumption without losing the register contents.

Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, where EXTI signal

The signals include one of 16 external I/O ports, PVD output, RTC alarm, Ethernet wake-up signal or USB wake-up signal.

l Standby mode In

this mode, the main LDO of the system is turned off, and the low-power LDO supplies power to the wake-up circuit. All other digital circuits are powered off, and FLASH is in a power-off state. Waking up the system from standby mode will generate a reset and SBF (PWR_CSR) will be set. After waking up, query the SBF status to know the low power consumption mode before waking up. SBF is cleared by the CSBF (PWR_CR) bit. In standby mode, the contents of the 32KB SRAM can be retained (depending on the planned configuration before sleep),

and the contents of the back-up registers are retained. Exit conditions: any external event (EXTI signal), external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, where the EXTI signal includes one of the 16 external I/O ports, RTC alarm clock, wake-up on Ethernet signal or USB wake-up signal.

2.5.7 CRC (Cyclic Redundancy Check) calculation unit The CRC

(Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In numerous applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting flash memory errors, a CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

2.5.8 Fast Programmable Interrupt Controller (PFIC) The

product has a built-in Fast Programmable Interrupt Controller (PFIC), which supports up to 255 interrupt vectors and provides flexible interrupt management functions with minimal interrupt delay. The current product manages 8 core private interrupts and 88 peripheral interrupt management, and other interrupt sources are reserved. The registers of the PFIC are accessible in both user

and machine privileged modes. l 2

independently maskable interrupts l Provide a

non-maskable interrupt NMI l Support hardware interrupt stack (HPE),

no instruction overhead l Provide 4-way table-

free interrupts (VTF) l Vector table supports address

or instruction mode l Interrupt nesting depth can be

Configure up to level 2 l to support the interrupt tail link function

2.5.9 External Interrupt/Event Controller (EXTI) The

external interrupt/event controller contains a total of 19 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured for its trigger event (rising edge or falling edge or both edges) and can be independently masked; the pending register maintains the status of all interrupt requests. EXTI can detect a pulse width smaller than the internal APB2 clock period. Up to 53 general-purpose I/O ports can be optionally connected to 16 external interrupt lines.

2.5.10 General DMA Controller

The system has a built-in general DMA controller that manages 8 channels, flexibly handles high-speed data transfers between memory and memory, peripherals and memory, and memory and peripherals, and supports the ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory, and can configure access priority, transfer length, source address and destination address of the transfer, etc.

DMA is used for major peripherals including: general/advanced/basic timers TIMx, ADC, USART, I2C, SPI.

Note: DMA accesses the system after arbitration by the arbitrator. CPU SRAM

2.5.11 Clock and startup

system clock source HSI is enabled by default. When no clock is configured or after reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 32MHz clock or PLL clock can be selected. When the clock safety mode is turned on, if the HSE is used as the system clock (directly or indirectly) and an external clock failure is detected at this time, the system clock will automatically switch to the internal RC oscillator, and the HSE and PLL will automatically shut down; for the low In power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled,

the software can receive the corresponding interrupt. Multiple prescalers are used to configure the frequency of AHB. The high-speed APB (APB2) and low-speed APE The frequency is 144MHz, refer to the clock tree block diagram in Figure 2-3.

2.5.12 RTC (Real Time Clock) and Backup Register

The RTC and backup registers are in the backup power supply area within the system. They are powered by VDD when VDD is valid. When VDD is invalid, the internal Switch to be powered by the VBAT pin.

The RTC real-time clock is a set of 32-bit programmable counters, and the time base supports 20-bit prescaler for measurement over a longer period of time. The clock reference source is a high-speed external clock divided by 128 (HSE/128), an external crystal low-frequency oscillator (LSE) or an internal low-power RC oscillator (LSI). LSE also has a backup power supply area, so when LSE is selected as the RTC time base, the RTC settings and time can remain unchanged after the system is reset or wakes up from standby mode. The backing register contains up to 42 16-bit

registers, which can be used to store 84 bytes of user application data. This data is on standby After waking up, or when the system is reset or the power is reset, it can continue to maintain. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

2.5.13 ADC (analog/digital converter) and touch key capacitance detection (TKey)

The product has a built-in 12-bit analog/digital converter (ADC), which can share up to 16 external channels and 2 internal channels for sampling. The programmable channel sampling time can realize single, continuous, scan or intermittent conversion, and supports dual ADC conversion mode. The analog watchdog function allows very accurate monitoring of one or more selected channels for monitoring channel signal voltage. Supports external event trigger conversion, and the trigger source includes the internal signal of the on-chip timer and the external pin. Supports the use of DMA operation.

The ADC internal channel sampling includes one built-in temperature sensor sampling and one internal reference power supply sampling. The temperature sensor generates a voltage that changes linearly with temperature. The temperature sensor is internally connected to the IN16 input channel, which converts the sensor output to a digital value. The

touch button capacitance detection unit provides up to 16 detection channels and multiplexes the external channels of the ADC module. The detection results are converted to output results through the ADC module, and the touch button status is identified through the user software.

2.5.14 Timer and Watchdog

Timers in the system include advanced timers, general timers, basic timers, watchdog timers and system time base timers.

Different products in the series contain different numbers of timers, please refer to Table 2-2 for details.

Table 2-2 Timer comparison

Timer resolution count type time base					DMA	function
advanced timer	TIM1	16 bit	up down up/down	APB2 time domain 16-bit frequency divider	support	PWM complementary output, single pulse output input capture Output Compare Timing Count
General timer	TIM2	16 bit	up down Up/Down	APB1 Time Domain 16-bit divider	support	input capture Output Compare Timing count
	TIM3					
	TIM4					
	TIM5	32 bit				
Window watchdog 7 bit down				APB1 time domain 4 crossovers	not support	timing Reset system (normal operation)
Independent watchdog 12-bit down				APB1 Time Domain 7 crossovers	not support	timing Reset system (normal + low power operation)
System time base timer 64 bit up or down				SYSCLK or SYSCLK/8	Timing is not supported	

l Advanced control timer The

advanced control timer is a 16-bit auto-loading up/down counter with a 16-bit programmable prescaler. Except for finishing
In addition to the general purpose timer function, it can be viewed as a three-phase PWM generator assigned to 6 channels, with complementary PWM with dead zone insertion.
Output functions that allow the timer to be updated after a specified number of counter cycles for repeated counting cycles, brake functions, etc. Advanced control
Many functions of timers are the same as general timers, and the internal structure is also the same, so advanced control timers can be linked through timers
The function operates in conjunction with other TIM timers to provide synchronization or event chaining capabilities.

l General timer

The general-purpose timer is a 16-bit or 32-bit autoloading up/down counter with a programmable 16-bit prescaler
And 4 independent channels, each channel supports input capture, output compare, PWM generation and single pulse mode output.
The timer chaining feature works with the advanced control timer to provide synchronization or event chaining capabilities. In debug mode, the counter can
The PWM outputs are disabled, thus turning off the switches controlled by these outputs. Any general purpose timer can be used to generate PWM
output. Each timer has an independent DMA request mechanism. These timers are also capable of processing incremental encoder signals and can also handle 1
Digital outputs to 3 Hall sensors.

l Independent watchdog

The independent watchdog is a free-running 12-bit down counter that supports 7 frequency division factors. consists of an internal independent 40KHz
An RC oscillator (LSI) provides the clock; because the LSI is independent of the main clock, it can operate in stop and standby modes. IWDG in main process
can work completely independently from the program and therefore be used to reset the entire system in the event of a problem or as a free timer for applications
The program provides timeout management. The watchdog can be configured to be software or hardware enabled through the option byte. In debug mode, the counter can
is frozen.

l Window watchdog

The window watchdog is a 7-bit down counter and can be set to free running. Can be used to reset the entire system in the event of a problem
system. It is driven by the main clock and has an early warning interrupt function; in debug mode, the counter can be frozen.

I System time base timer The

Qingke microprocessor core comes with a 64-bit optional increment or decrement counter, which is used to generate SYSTICK exceptions (exception number: 15). It can be used exclusively in real-time operating systems to provide a "heartbeat" rhythm for the system, and can also be used as a standard 64-bit counter. It has automatic reload function and programmable clock source.

2.5.15 Communication Interface

2.5.15.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The product provides 3 sets of universal synchronous/asynchronous receivers and transmitters (USART1, USART2, USART3), and 1 set of universal asynchronous receivers and transmitters (UART4). Supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-line communication. It also supports LIN (local interconnection network), is compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operate. Also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation for continuous comm

2.5.15.2 Serial Peripheral Interface (SPI)

Up to 2 sets of serial peripheral SPI interfaces, providing master or slave operation and dynamic switching. Supports multi-master mode, full-duplex or half-duplex synchronous transmission, and supports basic SD card and MMC modes. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, supports DMA operation for continuous communication.

2.5.15.3 I2C bus has up to 2

I2C bus interfaces, which can work in multi-master mode or slave mode and complete all I2C bus-specific timing, protocols, Arbitration, etc. Supports both standard and fast communication speeds and is compatible with SMBus2.0.

The I2C interface provides 7-bit or 10-bit addressing and supports dual slave addressing in 7-bit slave mode. Built-in hardware CRC generator It can use DMA operation and supports SMBus bus version 2.0/PMBus bus.

2.5.15.4 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), with a baud rate of up to 1Mbits/s and supports time-triggered communication. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers. It has 3 send mailboxes and 2 3-level deep receive FIFOs. There are only 14

settable filters for a CAN controller product with 1 group, and it shares a dedicated 512-byte SRAM memory with the USBD module for data transmission and reception. When USBD and CAN are used at the same time, in order to prevent access conflicts to SRAM, USBD can only use the lower 384-byte space.

2.5.15.5 Universal Serial Bus (USBD)

The product has a built-in USB2.0 full-speed controller and complies with the USB2.0 Fullspeed standard. USBD provides 16 configurable USB device endpoints, supports low-speed devices and full-speed devices, supports control/bulk/synchronous/interrupt transmission, double buffer mechanism, USB suspend/resume operation, and has standby/wake-up function. The USB-specific 48MHz clock is directly generated by the internal main PLL frequency division.

2.5.15.6 Universal Serial Bus USB2.0 Full Speed Host/Device Controller (USBFS)

USB2.0 Full-Speed Host Controller and Device Controller (USBFS) follows the USB2.0 Fullspeed standard. Provides 16 configurable USB device endpoints and a set of host endpoints. Supports control/batch/synchronous/interrupt transfer, double buffer mechanism, USB bus suspend/resume operation, and provides standby/wake-up function. The dedicated 48MHz clock of the USBFS module is directly generated by the internal main PLL frequency division (PLL must be 144MHz or 96MHz or 48MHz).

2.5.16 General Purpose Input/Output Interface (GPIO)

The system provides 4 groups of GPIO ports with a total of 53 GPIO pins. Each pin can be configured by software as an output (push-pull or open-drain), input (with or without pull-up or pull-down), or a multiplexed peripheral function port. Most GPIO pins are shared with multiplexed digital or analog peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. Provides a locking mechanism to freeze IO configuration,

This is to avoid accidental writing to I/O registers.

Most of the IO pin power in the system is provided by VIO. By changing the VIO power supply, the high value of the IO pin output level will be changed to adapt to the external Communication interface level. Please refer to the pin description for specific pins.

2.5.17 Operational Amplifier Comparator (OPA)

The product has two built-in op amp/comparator groups, which are internally selected to be associated with ADC and TIMx peripherals. Both input and output can be changed by changing the configuration It supports amplifying external analog small signals and sending them to ADC to realize small signal ADC conversion.

No. comparator function, the comparison result is output by GPIO or directly connected to the input channel of TIMx.

2.5.18 Serial 2-wire debug interface (SDI Serial Debug Interface)

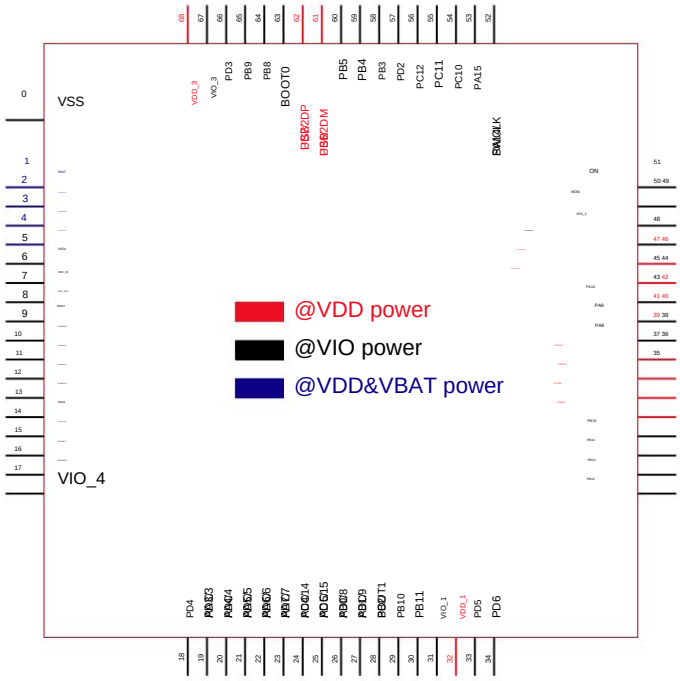
The core has a serial 2-wire debug interface (SDI), including SWDIO and SWCLK pins.

The test interface pin function is turned on, and SDI can be turned off as needed after the main program is run.

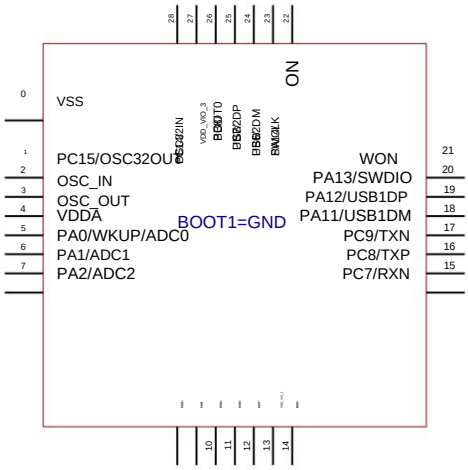
Chapter 3 Pin Information

3.1 Pinout

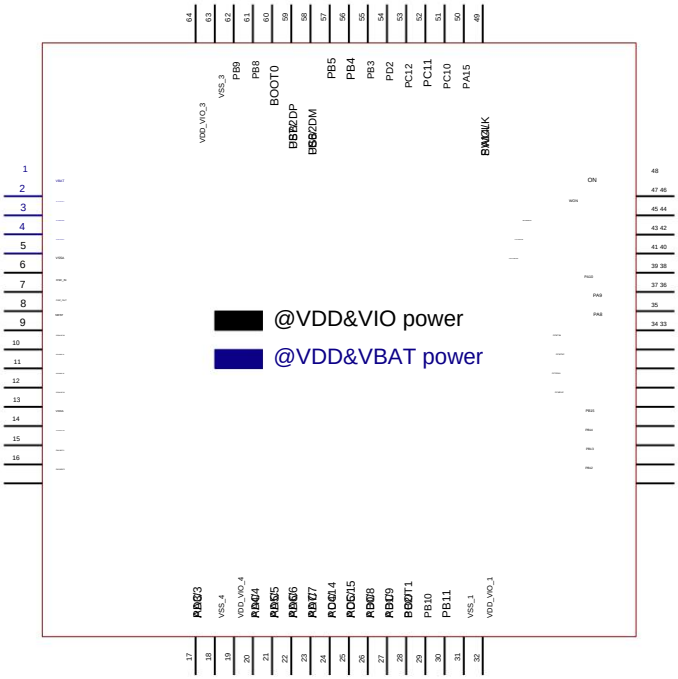
CH32V208WBU6



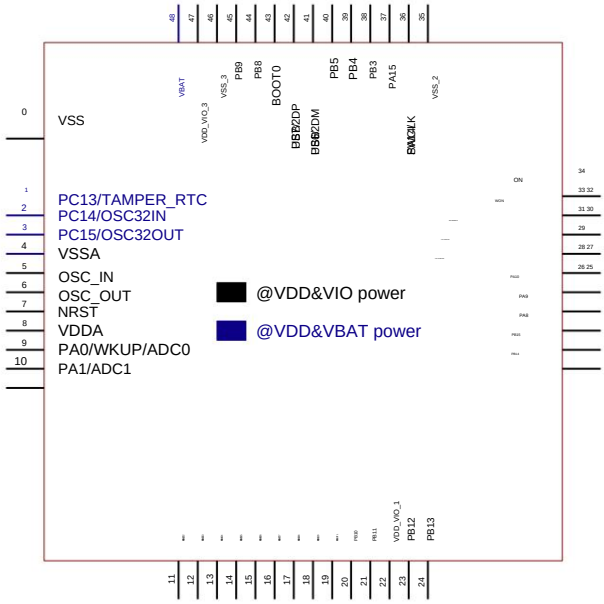
CH32V208GBU6



CH32V208RBT6



CH32V208CBU6



3.2 Pin Description

Table 3-1 Pin Definition

Note that the pin function descriptions in the following table are for all functions and do not involve specific model products. Peripheral resources vary between different models. Please confirm whether this function is available according to the product model resource table before checking.

Pin Number				pin name	Pinout type (1)	Ø electricity flat	Main Function (After reset)	Default multiplexing function	remapping function (8)
QFN28	QFN48	LQFP48	QFN68						
0	0	-	0	VSS	P		VSS		
-	48	1		VBAT	P		VBAT		
	1	2	2	PC13-TAMPER-RTC(2)	I/O -		PC13(3)	TAMPER-RTC	
28	2	3	3	PC14-OSC32_IN(2)	I/O/A -		PC14(3)	OSC32_IN	
1	3	4	4	PC15-OSC32_OUT(2)	I/O/A -		PC15(3)	OSC32_OUT	
-	4	5		VSSA	P		VSSA		
2	5	6	6	OSC_IN	I/A -		OSC_IN		
3	6	7	7	OSC_OUT	O/A -		OSC_OUT		
-	7	8	8	NRST			NRST		
-	-	9		PC0	I/O/A -		PC0	ADC_IN10	
-	-	10	10	PC1	I/O/A -		PC1	ADC_IN11	
-	-	11	11	PC2	I/O/A -		PC2	ADC_IN12	
-	-	12	12	PC3	I/O/A -		PC3	ADC_IN13	
4	8	13	13	VDDA	P		VDDA		
5	9	14	14	PA0-WKUP	I/O/A -		PA0	WKUP/USART2_CTS ADC_IN0/TIM2_CH1(9) TIM2_ETR(9)/TIM5_CH1	TIM2_CH1_2(9) TIM2_ETR_2(9)
6	10	15	15	PA1	I/O/A -		PA1	USART2_RTS/ADC_IN1 TIM5_CH2/TIM2_CH2	TIM2_CH2_2
7	11	16	16	PA2	I/O/A -		PA2	USART2_TX/TIM5_CH3 ADC_IN2/TIM2_CH3 OPA2_OUT0	TIM2_CH3_1
-	-	-	17	VIO_4	P		VIO_4		
-	-	-	18	PD4	I/O FT		PD4		
8	12	17	19	PA3	I/O/A -		PA3	USART2_RX/TIM5_CH4 ADC_IN3/TIM2_CH4 OPA1_OUT0	TIM2_CH4_1
-	-	18		VSS_4	P		VSS_4		
-	-	19	-	VDD_IO_4	P		VDD_IO_4		
9	13	20	20	PA4	I/O/A -		PA4	SPI1_NSS/USART2_CK ADC_IN4/OPA2_OUT1	
10	14	21	21	PA5	I/O/A -		PA5	SPI1_SCK/ADC_IN5	

Pin Number				Pinout name	pin type (1)	Ø electricity flat	Main Function (After reset)	Default multiplexing function remapping function (8)	
QFN28	QFN48	LQFP48	QFN68						
								OPA2_CH1N	
11	15	22	22	PA6	I/O/A	-	PA6	SPI1_MISO/ADC_IN6 TIM3_CH1/OPA1_CH1N	TIM1_BKIN_1
12	16	23	23	PA7	I/O/A	-	PA7	SPI1_MOSI/ADC_IN7 TIM3_CH2/OPA2_CH1P	TIM1_CH1N_1
-	-	24	24	PC4	I/O/A	-	PC4	ADC_IN14	
-	-	25	25	PC5	I/O/A	-	PC5	ADC_IN15	
-	17	26	26	PB0	I/O/A	-	PB0	ADC_IN8/TIM3_CH3 OPA1_CH1P	TIM1_CH2N_1 TIM3_CH3_2 UART4_TX_1
-	18	27	27	PB1	I/O/A	-	PB1	ADC_IN9 TIM3_CH4 OPA1_OUT1	TIM1_CH3N_1 TIM3_CH4_2 UART4_RX_1
-	19	28	28	PB2	I/O	FT	PB2/BOOT1		
-	20	29	29	PB10	I/O/A	FT	PB10	I2C2_SCL/USART3_TX OPA2_CH0N	TIM2_CH3_2 TIM2_CH3_3
-	21	30	30	PB11	I/O/A	FT	PB11	I2C2_SDA/USART3_RX OPA1_CH0N	TIM2_CH4_2 TIM2_CH4_3
-	-	31		VSS_1	P		VSS_1		
13	22	32	-	VDD_IO_1	P		VDD_IO_1		
-	-	-	31	VIO_1	P		VIO_1		
-	-	-	32	VDD_1	P		VDD_1		
-	-	-	33	PD5	I/O	FT	PD5		
-	-	-	34	PD6	I/O	FT	PD6		
-	23	33	35	PB12	I/O/A	FT	PB12	SPI2_NSS/I2C2_SMBA USART3_CK/TIM1_BKIN	
-	24	34	36	PB13	I/O/A	FT	PB13	SPI2_SCK/TIM1_CH1N USART3_CTS	USART3_CTS_1
-	25	35	37	PB14	I/O/A	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS/OPA2_CH0P	USART3_RTS_1
-	26	36	38	PB15	I/O/A	FT	PB15	SPI2_MOSI/TIM1_CH3N OPA1_CH0P	
14	-	37	39	PC6	I/O	FT	PC6	ETH_RXP	TIM3_CH1_3
15	-	38	40	PC7	I/O	FT	PC7	ETH_RXN	TIM3_CH2_3
16	-	39	41	PC8	I/O	FT	PC8	ETH_TXP	TIM3_CH3_3
17	-	40	42	PC9	I/O	FT	PC9	ETH_TXN	TIM3_CH4_3
-	27	41	43	PA8	I/O	FT	PA8	USART1_CK TIM1_CH1/MCO	USART1_CK_1 TIM1_CH1_1
-	28	42	44	PA9	I/O	FT	PA9	USART1_TX TIM1_CH2	TIM1_CH2_1

Pin number				pin name	Pinout type (1)	Ø electricity flat	Main Function (after reset)	Default reuse function	remapping function(8)
QFN28	QFN48	LQFP48	QFN68						
-	29	43	45	PA10	I/O FT		PA10	USART1_RX TIM1_CH3	TIM1_CH3_1
18	30	44	46	PA11	I/O A FT		PA11	USART1_CTS/USBDM CAN1_RX/TIM1_CH4	USART1_CTS_1 TIM1_CH4_1
19	31	45	47	PA12	I/O A FT		PA12	USART1_RTS/USBDP CAN1_TX/TIM1_ETR	USART1_RTS_1 TIM1_ETR_1
20	32	46	48	PA13	I/O FT		SWDIO		PA13
-	35	-	49	VSS_2	P		VSS_2		
21	33	47	50	WON	P		WON		
22	34	48	51	ON	A		ON		
23	36	49	52	PA14	I/O FT		SWCLK		PA14
-	37	50	53	PA15	I/O FT		PA15		TIM2_CH1_1(9) TIM2_ETR_1(9) TIM2_CH1_3(9) TIM2_ETR_3(9) SPI1_NSS_1
-	-	51	54	PC10	I/O FT		PC10	UART4_TX	USART3_TX_1
-	-	52	55	PC11	I/O FT		PC11	UART4_RX	USART3_RX_1
-	-	53	56	PC12	I/O FT		PC12		USART3_CK_1
-	-	54	57	PD2	I/O FT		PD2	TIM3_ETR	TIM3_ETR_2 TIM3_ETR_3
-	38	55	58	PB3	I/O FT		PB3		TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK_1
-	39	56	59	PB4	I/O FT		PB4		TIM3_CH1_2 SPI1_MISO_1
-	40	57	60	PB5	I/O FT		PB5	2C1_SMBA	TIM3_CH2_2 SPI1_MOSI_1
24	41	58	61	PB6	I/O FT		PB6	I2C1_SCL TIM4_CH1/USBFS_DM	USART1_TX_1
25	42	59	62	PB7	I/O FT		PB7	I2C1_SDA TIM4_CH2/USBFS_DP	USART1_RX_1
26(6)	43	60	63	BOOT0			BOOT0		
	44	61	64	PB8	I/O A FT		PB8	TIM4_CH3	I2C1_SCL_1 /CAN1_RX_2
-	45	62	65	PB9	I/O A FT		PB9	TIM4_CH4	I2C1_SDA_1 /CAN1_TX_2
-	-	-	66	PD3	I/O FT		PD3		
-	46	63	-	VSS_3	P		VSS_3		
27	47	64	-	VDD_IO_3	P		VDD_IO_3		

Pin Number				Pinout name	pin type (1)	I/O electricity flat	Main function (After reset)	Default multiplexing function	remapping function (8)
QFN28	QFN48	LQFP48	QFN68						
-	-	-	67	VIO_3	P		VIO_3		
-	-	-	68	VDD_3	P		VDD_3		

Note 1: Explanation of table abbreviations:

I = TTL/CMOS level Schmitt input; O = CMOS Level three-state output; A = Analog signal input or output;

P = power supply; 5V = 5V tolerant; = RF signal input and output (antenna);

ANT Note 2: PC13, PC14 and PC15 pins are powered through a power switch that can only sink a limited current (3mA).

PC13

Can be used as TAMPER pin, RTC alarm or seconds output; PC14 and PC15 can only be used as LSE pins;

When used as an output pin, it can only work in 2MHz mode, the maximum driving load is 30pF, and cannot be used as a current source (such as driving LED)

Note 8: The value after the underline of the remapping function indicates the configuration value of the corresponding bit in the register. For example: UART4_RX_0 means

The corresponding bit of the register is configured as 11b;

Note 9: TIM2_CH1 and ETR are the same pin, but cannot be used at the same time.

3.3 Pin alternate function

Note that the pin function descriptions in the table below are for all functions and do not involve specific models. Peripheral resources vary between different models. Please confirm whether this function is available according to the product model resource table before checking

Table 3-2 Pin multiplexing and remapping functions

Reuse / Pinout	ADC	TIM1	TIM2/3/4/5	UART/USART	USB	SYS	2C	SPI	ETH	OPA	CAN
PA0	ADC_IN0		TIM2_CH1 TIM2_ETR TIM2_CH1_2 TIM2_ETR_2 TIM5_CH1	USART2_CTS		BUY IN					
PA1	ADC_IN1		TIM2_CH2 TIM2_CH2_2 TIM5_CH2	USART2_RTS							
PA2	ADC_IN2		TIM2_CH3 TIM2_CH3_1 TIM5_CH3	USART2_TX						OPA2_OUT0	
PA3	ADC_IN3		TIM2_CH4 TIM2_CH4_1 TIM5_CH4	USART2_RX						OPA1_OUT0	
PA4	ADC_IN4			USART2_CK				SPI1_NSS		OPA2_OUT1	
PA5	ADC_IN5							SPI1_SCK		OPA2_CH1N	
PA6	ADC_IN6	TIM1_BKIN_1	TIM3_CH1					SPI1_MISO		OPA1_CH1N	
PA7	ADC_IN7	TIM1_CH1N_1	TIM3_CH2					SPI1_MOSI		OPA2_CH1P	
PA8		TIM1_CH1 TIM1_CH1_1		USART1_CK USART1_CK_1		MCO					
PA9		TIM1_CH2 TIM1_CH2_1		USART1_TX							
PA10		TIM1_CH3 TIM1_CH3_1		USART1_RX							
PA11		TIM1_CH4 TIM1_CH4_1		USART1_CTS USART1_CTS_1	USBDM						CAN1_RX
PA12		TIM1_ETR TIM1_ETR_1		USART1_RTS USART1_RTS_1	USBDP						CAN1_TX
PA13						SWDIO					
PA14						SWCLK					
PA15			TIM2_CH1_1 TIM2_ETR_1 TIM2_CH1_3 TIM2_ETR_3					SPI1_NSS_1			
PB0	ADC_IN8	TIM1_CH2N_1	TIM3_CH3 TIM3_CH3_2	UART4_TX_1						OPA1_CH1P	
PB1	ADC_IN9	TIM1_CH3N_1	TIM3_CH4 TIM3_CH4_2	UART4_RX_1						OPA1_OUT1	
PB2						BOOT1					
PB3			TIM2_CH2_1 TIM2_CH2_3					SPI1_SCK_1			
PB4			TIM3_CH1_2					SPI1_MISO_1			
PB5			TIM3_CH2_2				2C1_SMBA	SPI1_MOSI_1			
PB6			TIM4_CH1	USART1_TX_1	USBFS_DM		I2C1_SCL				
PB7			TIM4_CH2	USART1_RX_1	USBFS_DP		I2C1_SDA				
PB8			TIM4_CH3				I2C1_SCL_1				CAN1_RX_2
PB9			TIM4_CH4				I2C1_SDA_1				CAN1_TX_2

Reuse / Pinout	ADC	TIM1	TIM2/3/4/5	UART/USART	USB	SYS	2C	SPI	ETH	OPA	CAN
PB10			TIM2_CH3_2 TIM2_CH3_3	USART3_TX			I2C2_SCL			OPA2_CH0N	
PB11			TIM2_CH4_2 TIM2_CH4_3	USART3_RX			I2C2_SDA			OPA1_CH0N	
PB12		TIM1_BLOCK		USART3_CK			I2C2_SMBA	SPI2_NSS			
PB13		TIM1_CH1N		USART3_CTS USART3_CTS_1				SPI2_SCK			
PB14		TIM1_CH2N		USART3_RTS USART3_RTS_1				SPI2_MISO		OPA2_CH0P	
PB15		TIM1_CH3N						SPI2_MOSI		OPA1_CH0P	
PC0	ADC_IN10										
PC1	ADC_IN11										
PC2	ADC_IN12										
PC3	ADC_IN13										
PC4	ADC_IN14										
PC5	ADC_IN15										
PC6			TIM3_CH1_3						ETH_RXP		
PC7			TIM3_CH2_3						ETH_RXN		
PC8			TIM3_CH3_3						ETH_TXP		
PC9			TIM3_CH4_3						ETH_TXN		
PC10				UART4_TX USART3_TX_1							
PC11				UART4_RX USART3_RX_1							
PC12				USART3_CK_1							
PC13						TAMPER_RTC					
PC14						OSC32_IN					
PC15						OSC33_OUT					
PD2			TIM3_ETR TIM3_ETR_2 TIM3_ETR_3								

Chapter 4 Electrical Characteristics

4.1 Test conditions

Unless otherwise specified and noted, all voltages are referenced to VSS.

All minimum and maximum values are guaranteed under worst-case ambient temperature, supply voltage and clock frequency conditions. Typical values are base

It is used for design guidance **under normal temperature 25ÿ and VDD = 3.3V environment.**

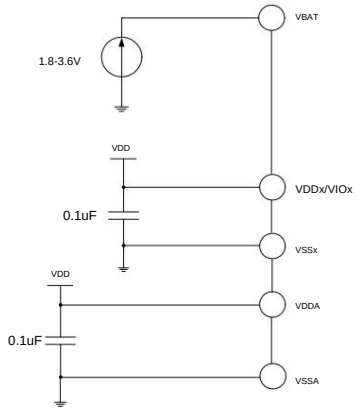
Data obtained through comprehensive evaluation, design simulation, or process characterization will not be tested on the production line.

Basically, the minimum and maximum values are obtained statistically after sample testing. Unless otherwise specified, these are actual measured values. Characteristic parameters are based on comprehensive evaluation.

or design warranty.

Power supply scheme:

Figure 4-1 Typical circuit of conventional power supply



4.2 Absolute maximum

Critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Table 4-1 Absolute maximum parameter table

Symbol	describe	Minimum	Maximum	Unit
TA working environment temperature		-40	85	ÿ
Ambient temperature during TS storage		-40	125 ÿ	
VDD-VSS External main power supply voltage (including VDDA and		-0.3	4.0	IN
VIO-VSS	VDD) IO domain supply	-0.3	4.0	IN
COME	voltage FT (5V tolerant) Input voltage on the pin	VSS-0.3	5.5	IN
	Input voltage on other pins |ÿVDD_x|	VSS-0.3	VDD+0.3	
Voltage difference between different main power supply pins |			50	mV
ÿVIO_x| Voltage difference between different IO supply pins |ÿVSS_x|			50	mV
Voltage difference between different ground pins			50	mV
VESD(HBM)	ESD electrostatic discharge voltage (human body model, non-contact)	4K		IN
	USB pins (PA11, PA12)	3K		IN
Total current of IVDD passing through VDD/VDDA/VIO power lines (supply current)			150	mA
IVssTotal current through VSS ground (source current) Sink			150	
IIO	current on any I/O and control pins Output current		25	
	on any I/O and control pins		-25	
IINJ(PIN)	NRST pin injects current		+/-5	

	HSE OSC_IN pin and LSE OSC_IN pin injection current Other pins		+/-5	
	injection current ÿIINJ(PIN)		+/-5	
Total injection current of all IO and control pins			+/-25	

4.3 Electrical parameters

4.3.1 Working conditions

Table 4-2 General working conditions

Symbol	Parameter	condition	Minimum value	Maximum value	unit
FHCLK	Internal AHB clock frequency			144	MHz
FPCLK1	Internal APB1 clock frequency			144	MHz
FPCLK2	Internal APB2 clock frequency			144	MHz
VDD	Standard operating voltage		2.4	3.6	IN
		Use USB or ETH	3.0	3.6	
VIO	Output voltage of most IO pins	VIO cannot be higher than VDD	2.4	3.6	IN
VDDA	analog part operating voltage (ADC is not used) VDDA must be the same as VIO , VREF+		2.4	3.6	IN
	Analog part operating voltage (using ADC)	Cannot be higher than VDDA, VREF-equal to VSS			
VBAT (1)	The backup unit operating voltage cannot be greater than VDD		1.8	3.6	IN
TA	Ambient temperature		-40	85	ÿ
TJ	Junction temperature range		-40	105 ÿ	

Note: 1. The connection between the battery and VBAT should be as short as possible.

Table 4-3 Power-on and power-off conditions

symbol	parameter	condition	Minimum value	Maximum value	unit
tVDD	VDD rise rate		0	ÿ	us/V
	VDD Falling Rate		30	ÿ	

4.3.2 Embedded reset and power control module features

Table 4-4 Reset and voltage monitoring (PDR selects high threshold gear)

symbol	Parameter conditions		Minimum value	Typical value	Maximum value	Unit
VPVD (1)	Programmable voltage detector Flat Selection	PLS[2:0] = 000 (rising edge)		2.39		IN
		PLS[2:0] = 000 (falling edge)		2.31		IN
		PLS[2:0] = 001 (rising edge)		2.56		IN
		PLS[2:0] = 001 (falling edge)		2.48		IN
		PLS[2:0] = 010 (rising edge)		2.65		IN
		PLS[2:0] = 010 (falling edge)		2.57		IN
		PLS[2:0] = 011 (rising edge)		2.78		IN
		PLS[2:0] = 011 (falling edge)		2.69		IN
		PLS[2:0] = 100 (rising edge)		2.89		IN
		PLS[2:0] = 100 (falling edge)		2.81		IN
		PLS[2:0] = 101 (rising edge)		3.05		IN
		PLS[2:0] = 101 (falling edge)		2.96		IN
		PLS[2:0] = 110 (rising edge)		3.17		IN
		PLS[2:0] = 110 (falling edge)		3.08		IN

		PLS[2:0] = 111 (rising edge)		3.31		IN
		PLS[2:0] = 111 (falling edge)		3.21		IN
VPVDhyst PVD hysteresis				0.08		IN
VPOR/PDR power-on/power-down reset threshold		rising edge	1.9	2.2	2.4	IN
		falling edge	1.9	2.2	2.4	IN
VPDRhyst PDR hysteretic				20		mV
tRSTTEMPO	power-on reset		24	28	30	mS
	other resets		8	10	30	

Note: 1. Test value at room temperature.

4.3.3 Built-in reference voltage

Table 4-5 Built-in reference voltage

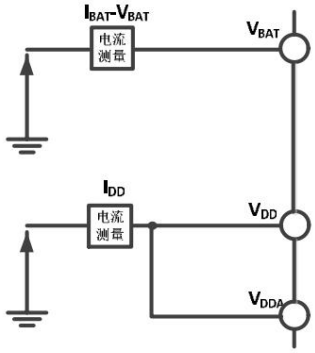
Symbolic parameters		condition	minimum value		Maximum value	unit
VREFINT built-in reference voltage		TA = -40ÿÿ85ÿ	1.17	1.2	1.23	IN
TS_vrefint	When reading the internal reference voltage When, the ADC sampling time				17.1	us

4.3.4 Supply current characteristics

Current consumption is a composite of multiple parameters and factors, including operating voltage, ambient temperature, I/O pin Load, software configuration of the product, operating frequency, I/O pin toggle rate, program location in memory, and executed code, etc.

The current consumption measurement method is as follows:

Figure 4-2 Current consumption measurement



The microcontroller is under the following conditions:

At room temperature , VDD = 3.3V, during the test: all IO ports are configured with pull-up input, only one of HSE or HSI is turned on, HSE = 32M, HSI=8M (calibrated), FPLCK1=FHCLK/2, FPLCK2=FHCLK, when FHCLK>8MHz, PLL is turned on. Enable or disable all peripheral clocks

Power consumption.

Table 4-6-1 Typical current consumption in run mode, data processing code runs from internal flash memory

symbol	parameter	condition		Typical value		unit
				Enable all peripherals	Disable all peripherals (2)	
IDD (1)	In run mode Supply current	external clock	FHCLK = 144MHz	21.37	16.77	mA
			FHCLK = 72MHz	10.91	8.73	
			FHCLK = 48MHz	7.58	6.16	
			FHCLK = 36MHz	6.49	5.29	
			FHCLK = 24MHz	4.59	3.61	

			FHCLK = 16MHz	3.13	2.59	
			FHCLK = 8MHz	2.0	1.71	
			FHCLK = 4MHz	1.42	1.28	
			FHCLK = 500KHz	1.0	0.95	
		Running on high-speed internal RC oscillator (HSI), Using AHB prescaler to reduce the frequency	FHCLK = 144MHz	20.75	16.27	
			FHCLK = 72MHz	10.74	8.53	
			FHCLK = 48MHz	7.42	5.98	
			FHCLK = 36MHz	5.96	5.05	
			FHCLK = 24MHz	4.62	3.41	
			FHCLK = 16MHz	3.03	2.49	
			FHCLK = 8MHz	1.66	1.42	
			FHCLK = 4MHz	1.11	1.0	
			FHCLK = 500KHz	0.63	0.62	

Note: 1. The above are actual measured parameters. 2. During testing, when all peripheral clocks are turned off, serial port 1 and GPIOA clock are not turned off.

Table 4-6-2 Bluetooth BLE power consumption

symbol	parameter		condition	Minimum value	Typical value	Maximum value	Unit
$I_{DD(BLE)}$ (1)	take over		Normal temperature VDD = 3.3V		15.2		mA
	send	-18dBm			6.28		
		0dBm			12.8		
		+7dBm			35.1		

Note: 1. The above are actual measured parameters.

Table 4-7 Typical current consumption in sleep mode, with data processing code running from internal Flash or SRAM

symbol	parameter	condition		Typical Value		unit
				Enable all peripherals	Disable all peripherals (2)	
I_{DD} (1)	In sleep mode Supply current (At this time, the peripherals supply Power and clock protection hold)	External clock	FHCLK = 144MHz	8.17	3.69	mA
			FHCLK = 72MHz	4.75	2.16	
			FHCLK = 48MHz	3.35	1.69	
			FHCLK = 36MHz	3.29	1.89	
			FHCLK = 24MHz	2.18	1.26	
			FHCLK = 16MHz	1.63	1.11	
			FHCLK = 8MHz	1.23	0.98	
			FHCLK = 4MHz	1.06	0.94	
			FHCLK = 500KHz	0.97	0.91	
		Running at high speed RC oscillator (HSI), Using AHB prescaler To reduce the frequency	FHCLK = 144MHz	7.65	3.44	
			FHCLK = 72MHz	4.61	2.02	
			FHCLK = 48MHz	3.22	1.55	
			FHCLK = 36MHz	2.73	1.44	
			FHCLK = 24MHz	1.9	1.1	
			FHCLK = 16MHz	1.48	0.95	
			FHCLK = 8MHz	0.93	0.69	

			FHCLK = 4MHz	0.75	0.63	
			FHCLK = 500KHz	0.58	0.56	

Note: 1. The above are actual measured parameters; 2. During the test, serial port 1, GPIOA clock, and power module clock were not turned off.

Table 4-8 Typical current consumption in stop and standby modes

symbol	parameter		Typical value units	
IDD	Supply current in stop mode	Conditional regulator is in run mode, low speed and high speed internal Both the RC oscillator and the external oscillator are turned off. status (no independent watchdog)	253.4	uA
		The voltage regulator is in low power mode, low speed and high speed internal Both the internal RC oscillator and the external oscillator are turned off. status (no independent watchdog, PVD off), RAM enters low power mode	23.8	
	Supply current in standby mode	The low speed internal RC oscillator and independent watchdog are at In the open state, all RAM is not powered	1.3	
		The low speed internal RC oscillator is turned on. The watchdog is turned off immediately, and all RAM is unpowered.	1.3	
		LSI/LSE/RTC/IWDG is turned off, 32K_RAM is powered and in low power state	2.18	
		LSI/LSE/RTC/IWDG is turned off, 2K_RAM is powered and in low power state	0.86	
		LSI/LSE/RTC/IWDG off, All RAM is unpowered	0.7	
IDD_VBAT	Supply current to backup area (Remove VDD and VDDA, only Powered by VBAT)	Low speed external oscillator and RTC are on	1.23	

Note: The above are actual measured parameters.

4.3.5 External clock source characteristics

Table 4-9 From external high-speed clock

symbolic parameters		condition	Minimum value	Typical value	Maximum value	Unit
FHSE_ext external clock frequency				32		MHz
VHSEH (1)	OSC_IN input pin high level voltage		0.8VIO		SAW	IN
VHSEL (1)	OSC_IN input pin low level voltage		0		0.2VIO	IN
Cin(HSE)	OSC_IN Input Capacitance			5		pF
DuCy(HSE) duty cycle				50		%
THE	OSC_IN Input Leakage Current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition errors.

Figure 4-3 External high-frequency clock source circuit

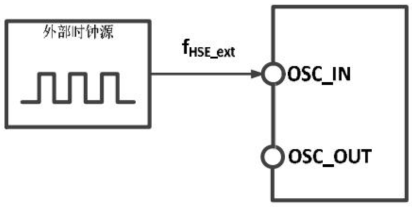


Table 4-10 From external low-speed clock

symbol	parameter	condition	Min Typ Max Unit			
FLSE_ext user	external clock frequency			32.768	1000	KHz
VLSEH	OSC32_IN input pin high level voltage		0.8VDD		VDD	IN
VLSEL	OSC32_IN input pin low level voltage		0		0.2VDD	IN
Eat (LSE)	OSC32_IN Input Capacitance			5		pF
DuCy(LSE) Duty	Cycle			50		%
THE	OSC32_IN Input Leakage Current				±1	uA

Figure 4-4 External low-frequency clock source circuit

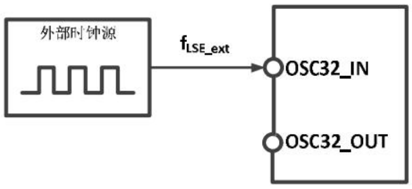


Table 4-11 High-speed external clock generated using a crystal/ceramic resonator

symbol	Parameter conditions		Minimum value Typical value Maximum value Unit			
FOSC_IN	resonator frequency			32(2)		MHz
RF	feedback resistor			250		kÿ
C	recommended load capacitance and corresponding crystal Series impedance RS	RS=60ÿ (1)		30		pF
I2	HSE Transconductance	VDD = 3.3V, 20p load start-up VDD		0.53		mA
tSU(HSE)	startup time of the driving	stable,		17.5		mA/V
	current gm oscillator	8M crystal		2.5		ms

Note: 1.25M is recommended. Not external load capacitor is ESR 60 2: Europe, lower than 25M It can be relaxed appropriately;

required.

Circuit reference design and requirements:

The load capacitance of the crystal shall be based on the recommendations of the crystal manufacturer. Normally, CL1=CL2.

The CH32V208x chip is connected to an external 32M crystal, and the chip has built-in load capacitors, so external circuits can be saved.

Figure 4-5 Typical circuit for external 32M crystal

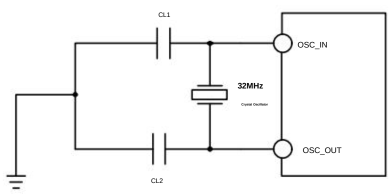


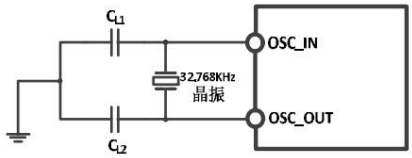
Table 4-12 Low-speed external clock generated using a crystal/ceramic resonator (fLSE=32.768KHz)

symbol	parameter	condition	Min Typ Max Unit			
RF feedback resistor				5		Mÿ
C	recommended load capacitance and corresponding crystal string Row impedance RS	RS<70kÿ			15	pF
i2	LSE Transconductance	VDD = 3.3V		0.35		uA
tSU(LSE) startup time	of the	start up		25.3		uA/V
driving current	gm oscillator	VDD is stable		800		mS

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the crystal manufacturer's recommendations. Normally CL1=CL2, the optional value is about 12pF.

Figure 4-6 Typical circuit for external 32.768K crystal



Note: The load capacitance CL is calculated by the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray is the capacitance of the pin and the board or PCB, the typical value of the related capacitor is between PCB 2pF-7pF.

4.3.6 Internal clock source characteristics

Table 4-13 High Speed Internal (HSI) RC Oscillator Characteristics

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
FHSI	frequency (after calibration)			8		MHz
DuCyHSI	duty cycle		45	50	55	%
ACCHSI	HSI oscillator accuracy (after calibration)	TA = 0ÿÿ70ÿ -1.0 TA = -40ÿÿ85ÿ -2.2			1.6	%
					2.2	%
tSU(HSI)	HSI oscillator startup settling time			10		us
IDD(HSI)	HSI Oscillator Power Consumption		120	180	270	uA

Table 4-14 Internal low-speed (LSI) RC oscillator characteristics

symbol	parameter	condition	Min Typ Max Unit			
FLSI	frequency		25	32	45	KHz
DuCyLSI	Duty Cycle		45	50	55	%
ACCLSI	LSI Oscillator Accuracy (After calibration)	Within ±1ÿ of constant temperature, 10s is recommended Calibrate once		±500		ppm
tSU(LSI)	LSI oscillator startup stabilization time			100		us
IDD(LSI)	LSI Oscillator Power Consumption			0.6		uA

4.3.7 PLL Characteristics

Table 4-15 PLL characteristics

symbol	parameter	condition	Min Typ Max Unit			
FPLL_IN	PLL Input Clock		4	8	25	MHz

	PLL input clock duty cycle		40		60	%
FPLL_OUT	PLL multiplied output clock		40		240(1)	MHz
tLOCK	PLL Lock Time				200	us

Note 1: An appropriate frequency multiplier must be selected to meet the output frequency range. PLL

4.3.8 Time to wake up from low power mode

Table 4-16 Low power mode wake-up time (1)

Symbol	parameter		Typical value	units
twusleep	wakes from sleep mode	Conditions Wake up from stop	2.6	us
twustop	mode using HSI RC clock wake up (regulator is in run mode)	HSI RC clock wake up	23.1	us
	Wake up from stop mode (regulator is in low power mode)	Regulator wake up time from low power mode + HSI RC clock wake-up	299	us
tWUSTDBY	wakes up from standby mode	LDO stabilization time + HSI RC clock wakeup + code loading time (2) (Example 128K)	5.0	ms

Note: 1. The above parameters are measured. 2. The code loading time is based on the current chip configuration. 0 *The waiting area capacity and loading configuration clock size can be calculated.*

4.3.9 Memory characteristics

Table 4-17 Flash memory characteristics

symbolic parameters		condition	Min	Typ	Max	Unit
Fprog	operating frequency (1)	TA = -40ÿÿ85ÿ			60	MHz
tprog_page	Page (256 bytes) Programming time	TA = -40ÿÿ85ÿ		2		ms
terase_page	Page (256 bytes) Erase time	TA = -40ÿÿ85ÿ		16		ms
terase_sec	Sector (4K bytes) Erase time	TA = -40ÿÿ85ÿ		16		ms
Vprog	programming voltage		2.4		3.6	IN

Note: 1. The operating frequency of flash includes reading, programming, and erasing, and the clock comes from HCLK.

Table 4-18 Flash memory life and data retention period

symbolic parameters		condition	Min	Typ	Max	Unit
NEND	number of erases	TA = 25ÿ	10K		80K(1)	Second-rate
tRET	and writes data retention period		20			Year

Note: The number of erase and write cycles is measured and not guaranteed.

4.3.10 I/O Port Characteristics

Table 4-19 General I/O static characteristics

symbol	parameter	Conditions	Min	Typ	Max	Unit
HIV	Standard I/O pin, input high level voltage		0.41*(VDD-1.8)+1.3		VDD+0.3	IN
	FT IO pin, input high level voltage		0.42*(VDD-1.8)+1		5.5	IN
WILL	Standard I/O pin, input low level voltage		-0.3		0.28*(VDD-1.8)+0.6	IN
	FT IO pin, input low level voltage		-0.3		0.32*(VDD-	IN

					1.8)+0.55	
Vhys	Standard I/O pin Schmitt trigger voltage hysteresis		150			mV
	FT IO pin Schmitt trigger voltage hysteresis		90			
Ilkg input leakage current		Standard IO ports			1	uA
		FT IO Ports			3	
RPU weak pull-up equivalent resistance			30	40	50	kÿ
RPD weak pull-down equivalent resistance			30	40	50	kÿ
CIO	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (general purpose input/output) ports can sink or source up to ±8mA, and sink or source ±20mA (not strictly

In user applications, the total current driven by all IO pins must not exceed the absolute maximum ratings given in Section 4.2 :

Table 4-20 Output voltage characteristics

symbol	parameter	condition	Minimum	Maximum	Unit
VOL	outputs low level, 8 pins absorb current	TTL port, IIO = +8mA		0.4	IN
VOH	outputs high level, 8 pins output current	2.7V< VDD <3.6V	VDD-0.4		
VOL	outputs low level, 8 pins absorb current	CMOS port, IIO = +8mA		0.4	IN
VOH	outputs high level, 8 pins output current	2.7V< VDD <3.6V	2.3		
VOL	outputs low level, 8 pins absorb current	IIO = +20mA		1.3	IN
VOH	outputs high level, 8 pins output current	2.7V< VDD <3.6V	VDD-1.3		
VOL	outputs low level, 8 pins absorb current	IIO = +6mA		0.4	IN
VOH	outputs high level, 8 pins output current	2.4V< VDD <2.7V	VDD-1.3		

Note: The above conditions may contain absolute maximum ratings in more than one section.

IO IO voltage, causing the drive current to be less than the nominal value

power/ ground point is very large, which will cause a voltage drop and the internal voltage will not reach the power supply voltage in the table.

Table 4-21 Input and output AC characteristics

MODEx[1:0] Configuration	symbol	parameter	condition	Minimum	Maximum	Unit
10 ÿ2MHzÿ	Fmax(IO)out	Maximum	CL=50pF,VDD=2.7-3.6V		2	MHz
	tf(IO)out	frequency Output high to low level fall time	CL=50pF,VDD=2.7-3.6V		125	ns
	tr(IO)out	output low to high level rising time			125	ns
01 ÿ10MHzÿ	Fmax(IO)out	maximum	CL=50pF,VDD=2.7-3.6V		10	MHz
	tf(IO)out	frequency output high to low level fall time	CL=50pF,VDD=2.7-3.6V		25	ns
	tr(IO)out	output low to high level rising time			25	ns
11 ÿ50MHzÿ	Fmax(IO)out	maximum frequency	CL=30pF,VDD=2.7-3.6V		50	MHz
			CL=50pF,VDD=2.7-3.6V		30	MHz
	tf(IO)out	output high to low level fall time	CL=30pF,VDD=2.7-3.6V		20	ns
			CL=50pF,VDD=2.7-3.6V		5	ns
	tr(IO)out	output low to high level rising time	CL=30pF,VDD=2.7-3.6V		8	ns
			CL=50pF,VDD=2.7-3.6V		12	ns
	tEXTIpw	EXTI controller detects external signal pulse width		10		ns

4.3.11 NRST pin characteristics

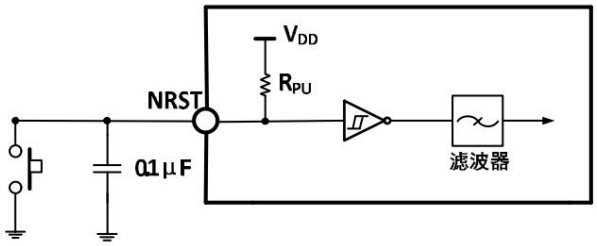
Table 4-22 External reset pin characteristics

Symbol parameter VIL(NRST)		condition	minimum value	Typical value	Maximum value unit	
NRST input low-level voltage VIH(NRST) NRST			-0.3		0.28*(VDD-1.8)+0.6V	
input high-level voltage NRST Schmitt trigger			0.41*(VDD-1.8)+1.3		VDD+0.3	IN
Vhys(NRST)	voltage Hysteresis		150			mV
RPU (1)	Weak pull-up equivalent resistance		30	40	50	kÿ
VF(NRST) NRST input can be filtered pulse width					100	ns
VNF(NRST) NRST input cannot filter pulse width			300			ns

Note: 1. The pull-up resistor is a real resistor in series with a switch. The resistance of this PMOS/ NMOS switch is very small (approximately accounts for 10%).

Circuit reference design and requirements:

Figure 4-7 Typical circuit of external reset pin



4.3.12 TIM timer characteristics

Table 4-23 TIMx features

symbol	parameter	condition	Minimum value	Maximum value	unit
tres(TIM) timer reference clock			1		tTIMxCLK
		fTIMxCLK = 72MHz	13.9		ns
FEXT	Timer external clock frequency for CH1 to CH4		0	fTIMxCLK/2	MHz
		fTIMxCLK = 72MHz	0	36	MHz
ResTIM timer resolution				16 bit	
tCOUNTER	When the internal clock is selected, the 16-bit count		1	65536	tTIMxCLK
	Clock cycle	fTIMxCLK = 72MHz	0.0139	910	us
tMAX_COUNT maximum possible count				65535	tTIMxCLK
		fTIMxCLK = 72MHz		59.6	s

4.3.13 I2C Interface Characteristics

Figure 4-8 I2C bus timing diagram

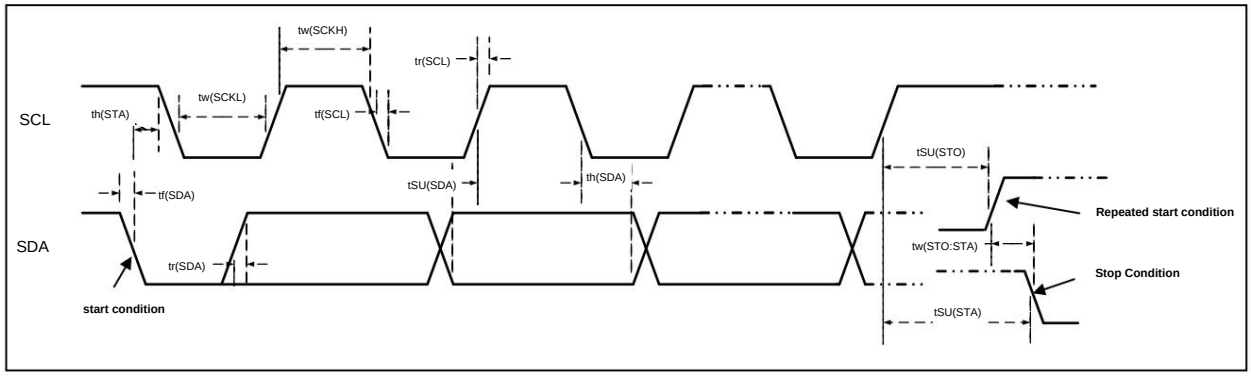


Table 4-24 I2C interface characteristics

symbol	parameter	Standard I2C		Fast I2C		unit
		Minimum	Maximum	Minimum	Maximum	
tw(SCKL)	SCL clock low time	4.7		1.2		us
tw(SCKH)	SCL clock high level time	4.0		0.6		us
tSU(SDA)	SDA data setup time	250		100		ns
th(SDA)	SDA data hold time	0		0	900	ns
tr(SDA)/tr(SCL)	SDA and SCL rise time tf(SDA)/		1000	20		ns
tf(SCL)	SDA and SCL fall time th(STA) Start		300			ns
	condition hold time tSU(STA) Repeated	4.0		0.6		us
	start condition setup time tSU(STO) Stop condition	4.7		0.6		us
	setup time tw(STO:STA) Stop condition to	4.0		0.6		us
	start condition time (bus idle) 4.7			1.2		us
Cb	Capacitive load of each bus		400		400	pF

4.3.14 SPI interface characteristics

Figure 4-9 SPI master mode timing diagram

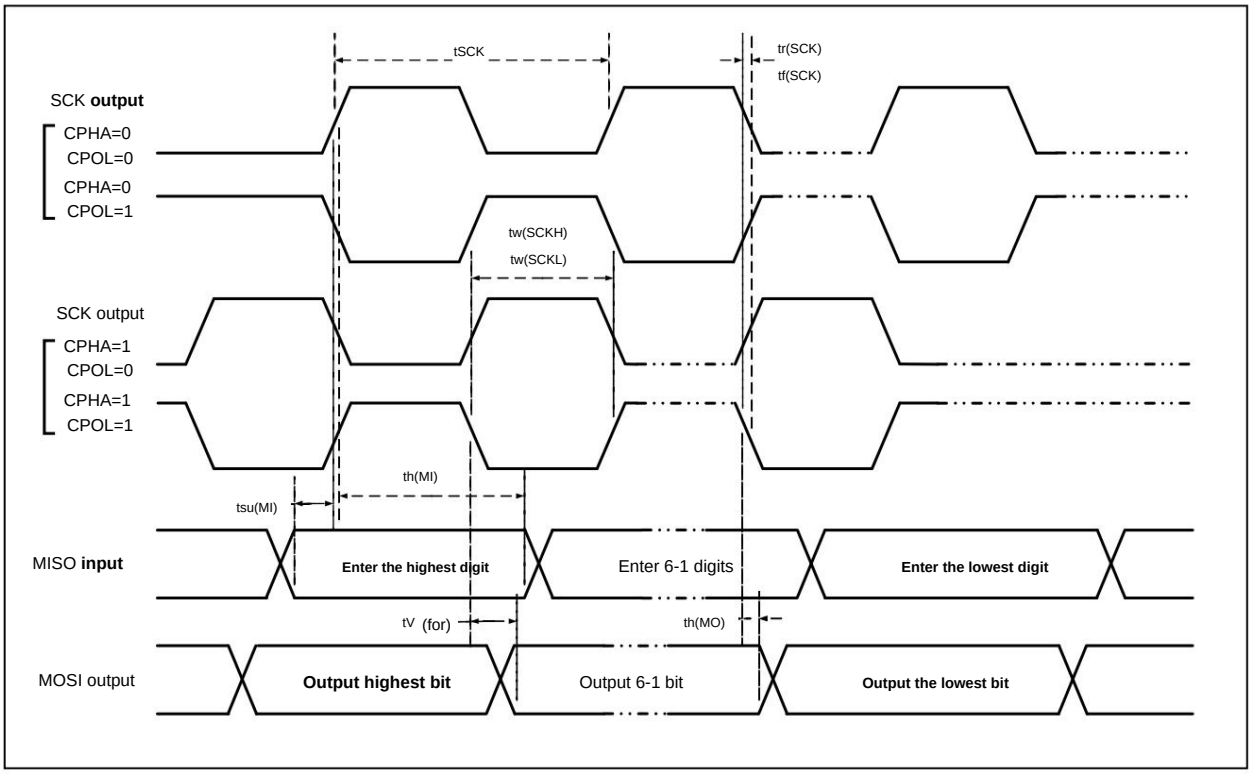


Figure 4-10 SPI slave mode timing diagram (CPHA=0)

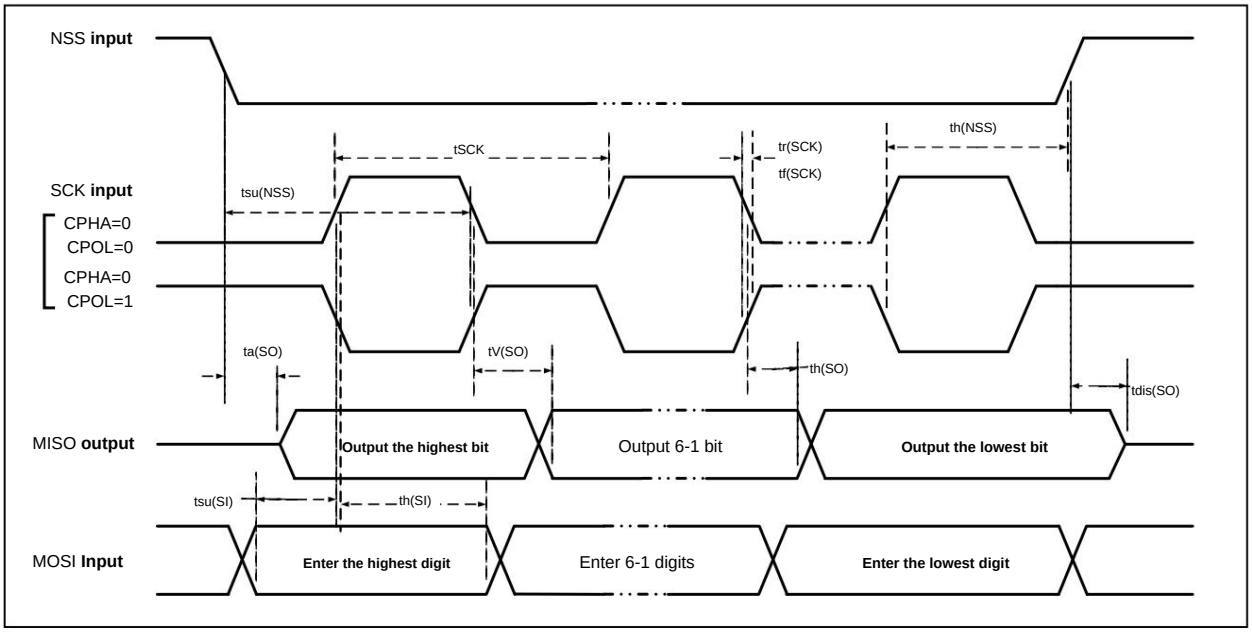


Figure 4-11 SPI slave mode timing diagram (CPHA=1)

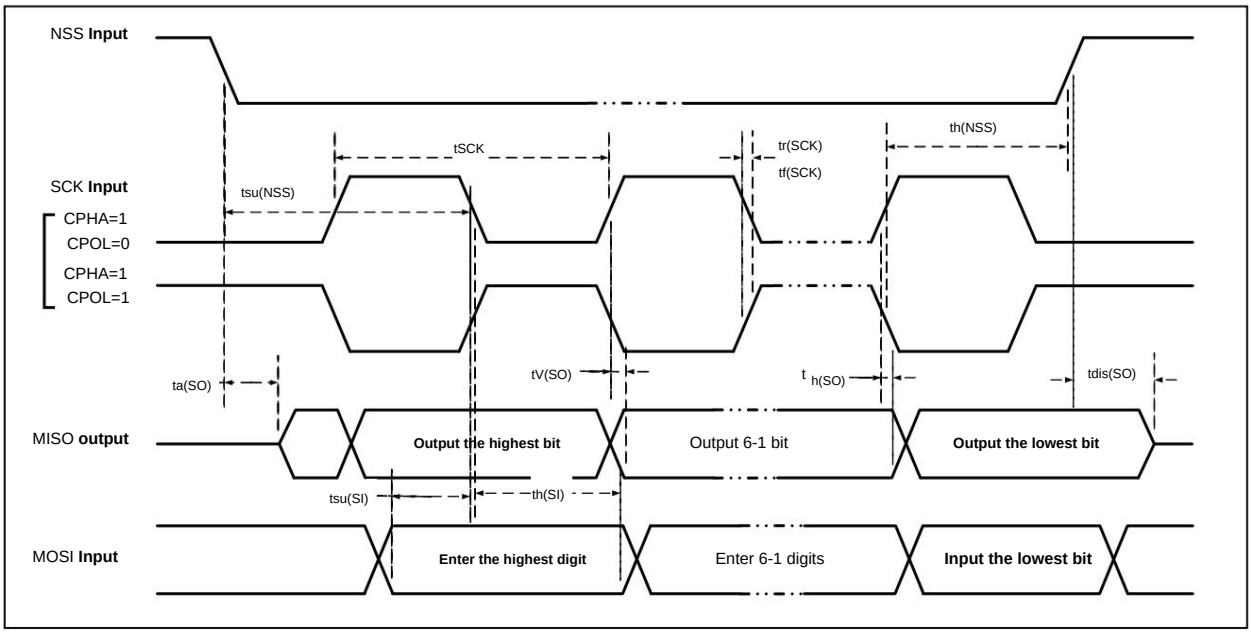


Table 4-25 SPI interface characteristics

symbol	parameter	condition	Minimum Maximum Unit		
fSCK/tSCK	SPI clock frequency	Master		36	MHz
		mode		36	MHz
Slave mode tr(SCK)/tf(SCK) SPI clock rise and fall time Load capacitance: C = 30pF				20	ns
tSU(NSS)	NSS establishment time	Slave	2tPCLK		ns
th(NSS)	NSS hold time	mode	2tPCLK		ns
tw(SCKH)/tw(SCKL) SCK high level and low level time		Slave mode Master mode, fPCLK = 36MHz, prescaler Coefficient	40	60	ns
tSU(MI)	Data entry setup time	= 4 Master	5		ns
tSU(SI)		mode	5		ns
th(MI)	Data input hold time	Slave	5		ns
th(SI)		mode	4		ns
ta(SO) data output access time tdis(SO) data		Master mode Slave mode Slave	0	1tPCLK	ns
output disable time		mode,	0	10	ns
tV(SO)	Data output valid time	fPCLK = 20MHz Slave mode Slave		25	ns
tV(MO)		mode (after enable edge) Master mode		5	ns
th(SO)	Data output hold time	(after enable edge) Slave mode (after	15		ns
th(MO)		enable edge) Master mode (after enable edge))	0		ns

4.3.15 USB interface characteristics

Table 4-26 USB module characteristics

symbol	parameter	condition	Minimum value	Maximum value	unit
VDD	USB operating voltage		3.0	3.6	IN
VSE single-ended receiver threshold		VDD = 3.3V	1.2	1.9	IN
VOL static output low level				0.3	IN
VOH static output high level			2.8	3.6	IN

VHSSQ high-speed suppression information detection threshold		100	150	mV
VHSDSC High Speed Disconnect Detection Threshold		500	625	mV
VHSOI high speed idle level		-10	10	mV
VHSOH High speed data high level		360	440	mV
VHSOL High speed data low level		-10	10	mV

4.3.16 12-bit ADC Characteristics

Table 4-27 ADC characteristics

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
VDDA	supply voltage		2.4		3.6	IN
VREF+	positive reference voltage	VREF+ cannot be higher than VDDA	2.4		VDDA	IN
IVREF	reference current			160	220	uA
IDDA	supply current			480	530	uA
fADC	ADC clock frequency				14	MHz
fS	sampling rate fTRIG		0.05		1	MHz
	external trigger frequency				16	1/fADC
VAIN	conversion voltage range		0		VREF+	IN
RAIN	External input impedance				50	kÿ
RADC	sampling switch resistance			0.6	1	kÿ
CADC	internal sampling and holding capacitor			8		pF
tCAL	calibration time tlat			40		1/fADC
	injection trigger conversion delay tlatr				2	1/fADC
	conventional trigger conversion delay ts				2	1/fADC
	sampling time tSTAB power-		1.5		239.5 1/fADC	
	on time tCONV total				1	us
	conversion time (including sampling time)		14		252	1/fADC

Note: The above are all guaranteed design parameters.

Official: Max RAIN

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. Where N=12 (meaning 12-bit resolution).

Table 4-28 Maximum **RAIN when fADC** = 14MHz

TS(period)	tS (us)	Maximum RAIN(kÿ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	invalid
239.5	17.1	invalid

Table 4-29 ADC error

symbol	parameter	condition	Min	Typ	Max	Unit
EO	offset error	fPCLK2 = 56 MHz,fADC =		±2		
ED	Differential nonlinearity error	14 MHz,RAIN < 10		±0.5	±3	LSB
EL	Integral nonlinearity error	kÿ,VDDA = 3.3V		±1	±4	

Cp represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger Cp value will

To reduce the conversion accuracy, the solution is to reduce the fADC value.

Figure 4-12 ADC typical connection diagram

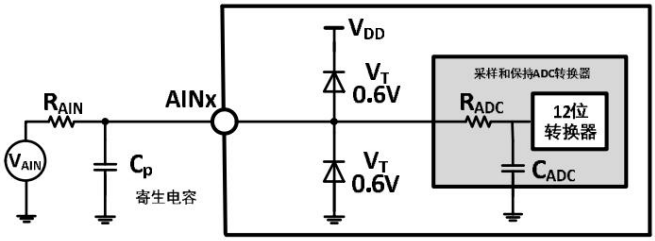
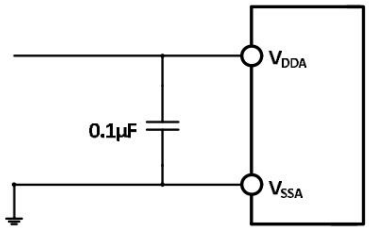


Figure 4-13 Analog power supply and decoupling circuit reference



4.3.17 Temperature sensor characteristics

Table 4-30 Temperature sensor characteristics

Symbolic parameters		condition	Minimum value	Typical value	Maximum value	Unit
RTS	temperature sensor measurement range		-40		85	ÿ
Measurement Error of	ATSC Temperature Sensor			±12		ÿ
Avg_Slope	Average slope (negative temperature coefficient)		3.8	4.3	4.8	mV/ÿ
V25	voltage at 25°C		1.34	1.40	1.46	IN
TS_temp	When reading temperature, ADC sampling time fADC = 14MHz				17.1	us

4.3.18 OPA features

Table 4-31 OPA characteristics

symbol	parameter	condition	Min	Typ	Max	Unit
VDDA	supply voltage		2.4	3.3	3.6	IN
CMIR	common mode input voltage		0		VDDA-0.9	IN
VIOFFSET	input offset voltage			2.5	8	mV
ILOAD	drive current				600	uA
IDDOPAMP	Current consumption	No load, static mode		195		uA
CMRR (1)	Common-mode	@1KHz		96		dB
PSRR (1)	rejection ratio Power	@1KHz		86		dB
OF (1)	supply rejection ratio Open-loop gain	CLOAD=5pF		136		dB

GBW(1)	Unity gain bandwidth	CLOAD=5pF		19		MHz
PM(1)	Phase margin	CLOAD=5pF		93		
SR(1)	Slew rate	CLOAD=5pF P		8		V/us
tWAKU(1)	shutdown to wake-up setup time, 0.1% input VDDA/2, CLOAD=5pF, RLOAD=4kÿ RLOAD resistive load				368	ns
			4			kÿ
CLOAD Capacitive load					50	pF
VOHSAT(2)	High saturation output voltage	RLOAD=4kÿ, input VDDA	VDDA-45			mV
		RLOAD=20kÿ, input VDDA VDDA-10				
WANTED(2)	Low saturation output voltage	RLOAD=4kÿ, input 0			0.5	mV
		RLOAD=20kÿ, input 0			0.5	
EN(1) equivalent input voltage noise		RLOAD=4kÿ,@1KHz		83		$\frac{nv}{\sqrt{Hz}}$
		RLOAD=4kÿ,@10KHz		42		

Note: 1. The source is simulation, not actual measurement; 2. The load current will limit the saturated output voltage.

Chapter 5 Packaging and Ordering Information

Chip packaging

Ordering model	package type	plastic body width	pin spacing	Packaging instructions	Shipping
CH32V208GBU6	QFN28X4	4*4mm	tray 0.4mm	28-pin pallet with no leads on four sides	
CH32V208CBU6	QFN48X5	5*5mm	0.35mm	48-pin pallet with no leads on four sides	
CH32V208RBT6	LQFP64M	10*10mm	0.5mm	LQFP64M (10*10) SMD tray	
CH32V208WBU6	QFN68X8	8*8mm	0.4mm	4-side leadless 68-pin tray	

Note: 1.QFP/QFN generally defaults to pallet.

2. Pallet size: The pallet size is generally uniform, 322.6*135.9*7.62, and the limit hole sizes of different package types are different.

There are differences in plastic tube packaging between different factories, please confirm with the manufacturer for details.

Note: The dimension unit is mm (millimeters). The center spacing of the pins is always the nominal value and there is no error. Other dimensional errors are not Greater than ±0.2mm or ±10%, whichever is greater.

Figure 5-1 QFN28X4 package

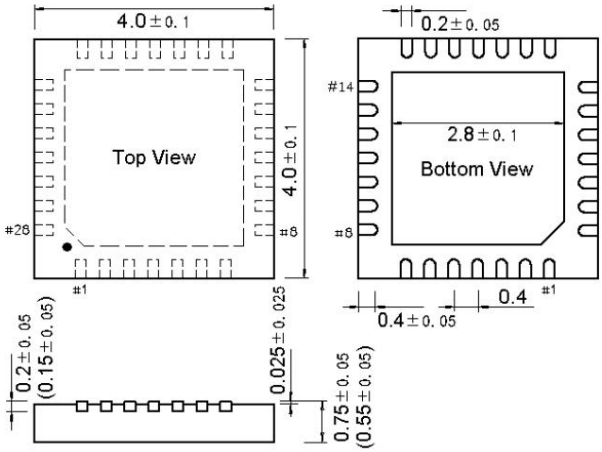


Figure 5-2 QFN48X5 package

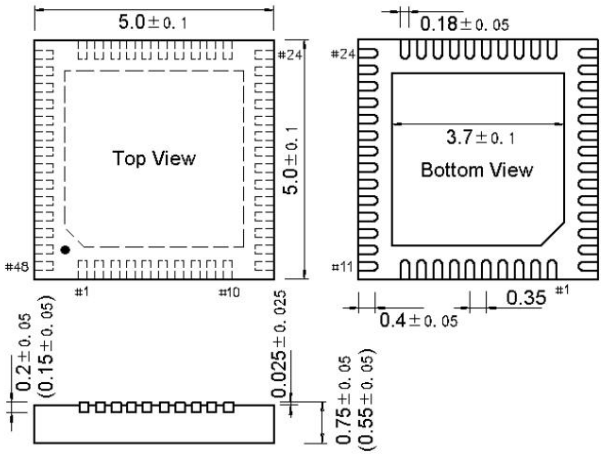


Figure 5-3 QFN68X8 package

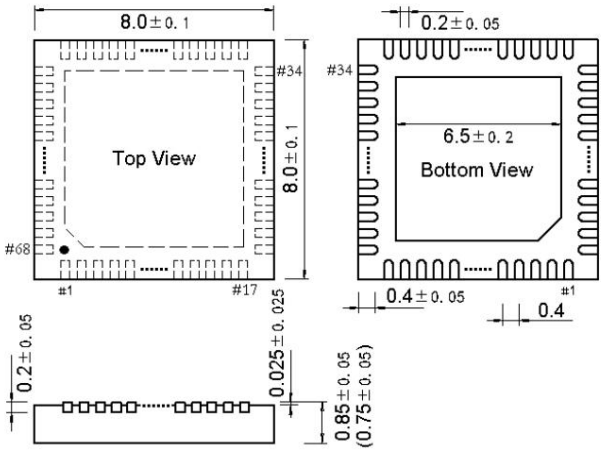
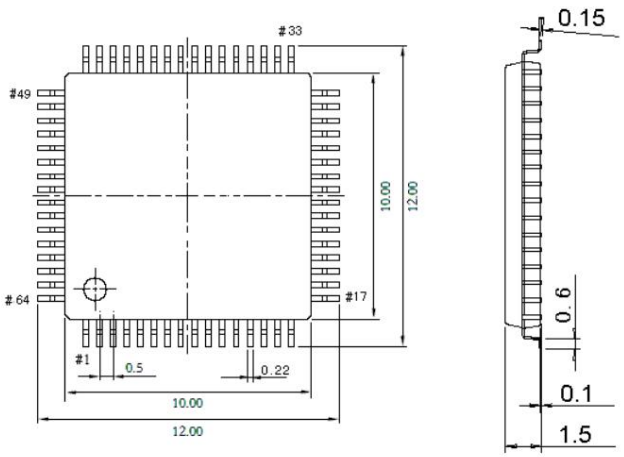


Figure 5-4 LQFP64M package



Series product naming rules

Example: CH32 IN 3 03 R 8 T 6

Product Series

F = Based on ARM core, general purpose MCU

V = Based on Qingba RISC-V core, general-purpose MCU

L = Based on Qingba RISC-V core, low-power MCU

X = Based on Qingke RISC-V core, dedicated architecture or special IO

product type

0 = Qingke V2/V4 kernel, main frequency @48M

1 = M3/Highland Barley V3/V4 core, main frequency @72M

2 = M3/Qingke V4 non-floating point core, main frequency @

144M 3 = Qingke V4F floating point core, main frequency @ 144M

Product Sub-Series

03 = Universal

05 = Connected type (USB high-speed, SDIO, dual CAN)

07 = Interconnected type (USB high-speed, dual CAN, Ethernet, SDIO, FSMC)

08 = Wireless type (Bluetooth BLE5.X, CAN, USB, Ethernet)

35 = Connected (USB, USB PD)

Number of pins

J = 8 pins A = 16 pins F = 20 pins

G = 28 pins K = 32 pins T = 36 pins

C = 48 feet R = 64 feet W = 68 feet

V = 100 pin Z = 144 pin

Flash storage capacity

4 = 16K flash memory

6 = 32K flash memory

7 = 48K flash memory

8 = 64K Flash memory

B = 128K flash memory

C = 256K flash memory

Encapsulation

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

temperature range

6 = -40ÿÿ85ÿÿindustrial gradeÿ

7 = -40ÿÿ105ÿ (automotive grade 2)

3 = -40ÿÿ125ÿ (automotive grade 1)

D = -40ÿÿ150ÿ (automotive grade 0)