Product Manual

ECK20-6Y2XA

Chengdu Ebyte Electronic Technology Co.,Ltd.

Contents

Disclaimer

The information in this document is subject to change without notice. The document is provided "as is" without any warranty, including any warranty of merchantability, fitness for a particular purpose or non-infringement, and any warranty mentioned elsewhere in any proposal, specification or sample. This do cument does not assume any responsibility, including liability for infringement of any patent rights arising from the use of the information in this document. This document does not grant any intellectual property rights license by estopp el or otherwise, whether express or implied.

The test data obtained in this article are all obtained by Ebyte laboratory testing, and the actual results may be slightly different.

All trade names, trademarks and registered trademarks mentioned in this ar ticle are the property of their respective owners, and are hereby declared.

The final right of interpretation belongs to Chengdu Ebyte Electronic Tech nology Co., Ltd.

Notice:

Due to product version upgrades or other reasons, the contents of this manual may change. Ebyte El ectronic Technology Co., Ltd. reserves the right to modify the contents of this manual without any notice or reminder. This manual is only used as a guide. Chengdu Ebyte Electronic Technology Co., Ltd. tries its best to provide accurate information in this manual, but Chengdu Ebyte Electronic Technology Co., Lt d. does not ensure that the contents of the manual are completely error-free, and all statements, informati on and suggestions in this manual do not constitute any express or implied warranty.

1 Product Overview

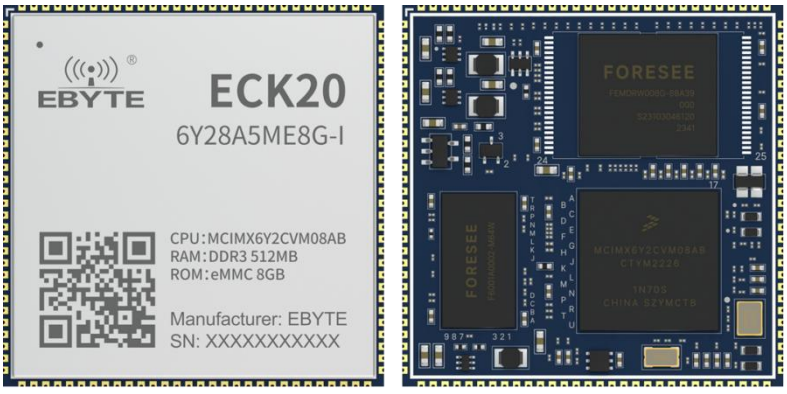
1.1.Product introduction

Ebyte ECK20-6Y2XA series core board is carefully designed based on NXP Cortex-A7 core i.MX6ULL processor, and is a low-cost, low-power, cost-effective, and highly reliable embedded core board connected by stamp holes. It can be widely used in industrial control, HMI, IoT and other fields.

NXP's i.MX6ULL processor uses a single ARM Cortex-A7 core with a maximum main frequency of 792MHz. It can provide rich I/O resources such as 1 LCD display, 1 digital camera, 2 100M Ethernet, 2 USB OTG, 8 UART, 2 SDIO, 2 CAN, multiple GPIO, etc.

The ECK20-6Y2XA series core board includes 3 specific product models. They mainly have some differences in memory capacity, storage configuration, etc. Customers can choose the appropriate model according to their needs. For product selection, please refer to the product selection section.

The physical picture of the ECK20-6Y2XA series core board (without components on the bottom of the product) is as follows:



Physical picture

1.2.Features

1、Processor: i.MX6ULL series industrial-grade processor, main frequency 792MHz;

2、Memory: On-board DDR3L SDRAM, 256MB/512GB capacity optional;

3、Storage: 8GB eMMC or 512MB parallel NAND FLASH optional;

4、Display: 1 parallel display interface, maximum resolution supports WXGA (1366×768@

60fps);

5、Network: 10/100 adaptive Ethernet MII/RMII interface;

6、USB: 2-way USB2.0 OTG interface;

7、SDIO: 2-way MMC/SD/SDIO card interface (eMMC configuration only supports 1-way SDIO lead-out);

8、Multiple extended I/O interfaces: including UART, CAN, I2C, SPI, SAI, ADC, GPIO, etc.

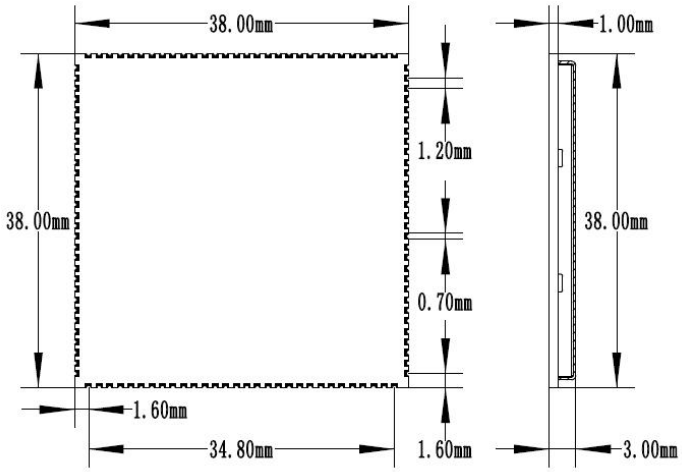
9、Supports on-chip watchdog function (timeout can cause processor reset);

10、Support on-chip RTC function;

11、Interface type: 120-pin stamp hole;

12、Power supply: single-channel DC +5V±10%@0.3A power input;

13、Structural dimensions: 38×38× 3mm , as shown in the following figure:

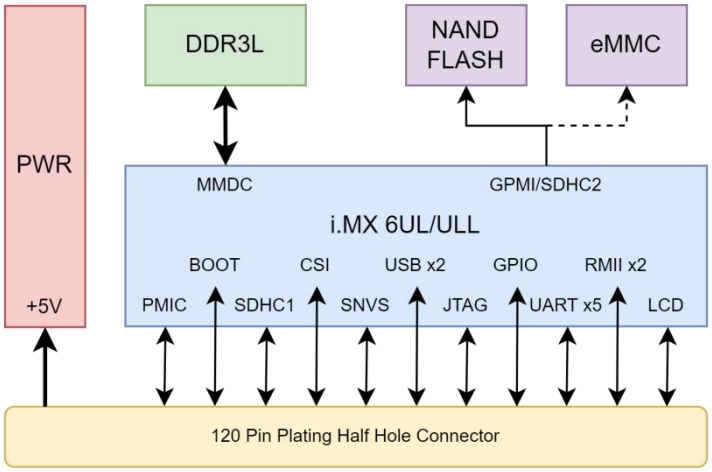


Dimensions

14、Working temperature: Commercial grade: 0℃-70℃, Industrial grade: -40℃-85℃;

15、PCB technology: 8-layer board design, immersion gold, lead-free technology;

1.3.Core board functional block diagram



Functional Block Diagram

1.4.Typical applications

- Smart home;
- Smart toys;
- Smart cities;
- Tablet computer;
- IoT Gateway;
- Advertising all-in-one machine;
- Industrial all-in-one machine;
- Industrial control motherboard;
- Robots and drones.

2. Product Selection

2.1.Model configuration

The ECK20-6Y2XA series core board selection and configuration table is as follows:

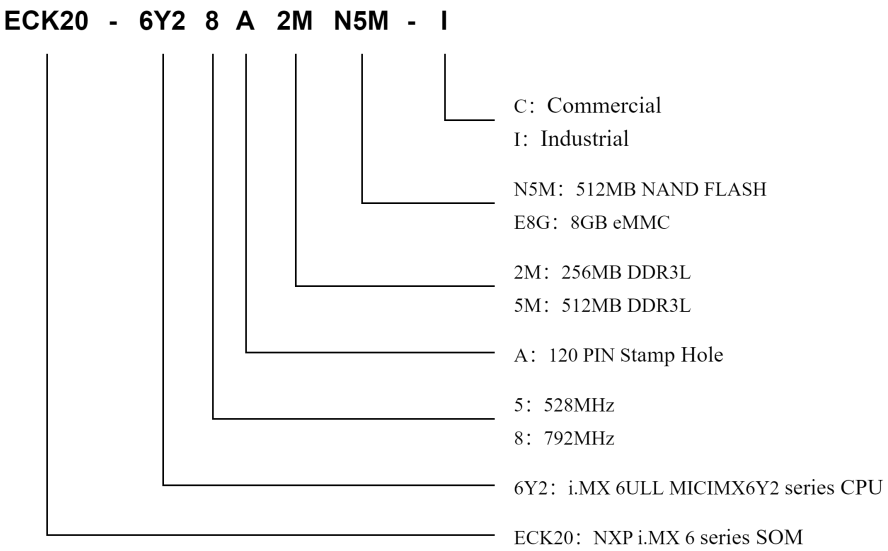
Product Selection and Configuration Table

Serial number	Product Model	Processor model	Memory	storage	Operating temperature
1	ECK20-6Y28A2MN5M-I	MCIMX6Y2CVM08AB	256MB	512MB	Industrial Grade

			DDR3L	NAND	-40℃ ~ 85℃
2	ECK20-6Y28A5ME8G-C	MCIMX6Y2CVM08AB	512MB DDR3L	8GB eMMC	Commercial Grade 0℃ ~ 70℃
3	ECK20-6Y28A5ME8G-I	MCIMX6Y2CVM08AB	512MB DDR3L	8GB eMMC	Industrial Grade -40℃ ~ 85℃

2.2.Model code

The product model coding is shown in the figure below:



Model code description

3. Quick Experience

Choosing Ebyte single board computer products, you can quickly experience the typical application functions, baseboard design, software development, etc. of ECK20-6Y2XA core board products.

4. Features and Parameters

4.1.Product features

The ECK20-6Y2XA series core board mainly integrates the processor, memory, storage an

d power system, and leads out all the I/O pins on the processor. Users can design the baseboa rd to apply the I/O resources on the core board according to their needs and reuse the I/O int o the functions they need.

The following table lists the main function parameters of the ECK20-6Y2XA series core b oard integrated on the board, and the function parameters of the reusable I/O resources. The d escription of each I/O function is the maximum indicator that the core board can use the I/O function without using other I/O functions (for example, after using 1 24-bit color LCD interfa ce function and 2 network interface functions, 8-way UART function cannot be realized).

Product Features

product	Functional Description	
processor	MCIMX6Y2CVM08AB; i.MX 6ULL Applications Processors for Industrial; Single Arm Cortex-A7 core, 792MHz;	
storage	Memory	On-board DDR3L SDRAM, 16-bit width, 256MB/512MB optional;
	FLASH	On-board 8GB eMMC / on-board 512MB parallel NAND FLASH optional;
show	1 parallel display interface, maximum resolution supports WXGA (1366×768@60fps); Support 24bit, 18bit, 16bit, 8bit parallel display output;	
Camera	1 parallel camera interface, supporting up to 24-bit data and 85MHz clock; Support 24bit, 16bit, 10bit, 8bit data input; Support BT.656 data format;	
USDHC	2-way MMC/SD/SDIO card interface; 1-bit or 4-bit SD/SDIO card, up to UHS-I SDR-104 mode; 1bit, 4bit or 8bit mode MMC card, maximum support DDR mode; 4-bit or 8-bit mode eMMC, supporting up to HS200 mode;	
USB	2-way USB 2.0 OTG;	
Audio	3-way I2S/SAI/AC97, maximum 1.4Mbps per way; Support ESAI audio interface; Support SPDIF audio interface;	
Serial Port	8-channel UART, maximum 5Mbps per channel;	
SPI	4-channel eCSPI (Enhanced CSPI), maximum 52Mbps per channel;	
Ethernet	2-way 10/100 Ethernet MAC, support IEEE1588, support RMII;	
I2C	4-way I2C, maximum 400Kbps per channel;	
CAN	2-way CAN interface, supporting CAN 2.0B protocol;	
PWM	8-channel PWM, maximum clock frequency 66MHz;	
ADC	2 12-bit ADCs, supporting up to 10 input channels;	
EIM	Support EIM (External Interface Module), expandable NOR FLASH or PSRAM, etc.;	
JTAG	Support System JTAG Controller;	
TIMER	2 GPT (General Purpose Timer) timer functions;	
WDT	3 Watchdog timer functions;	
keyboard	1 8×8 matrix keyboard function;	

GPIO	105 (maximum) GPIO, supporting interrupt function;

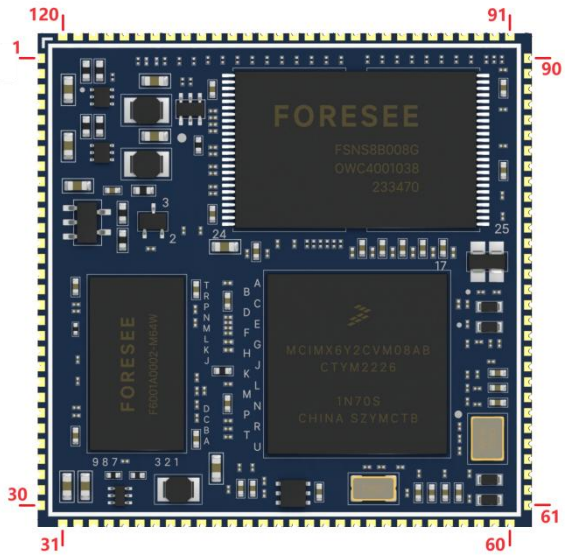
4.2.Environmental characteristics

Environmental characteristics table

Operating temperature	Commercial Grade	0℃ ~ 70℃;
	Industrial Grade	-40℃ ~ 85℃;
Storage temperature	-40 ~ 85℃;	
Operating humidity	5~95% humidity, non-condensing;	
Storage humidity	60℃@95% humidity, non-condensing;	

4.3.I/O features

4.3.1. I/O Pin definition



Pin Number Diagram

Pin Definition Table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
1	CSI_VSYNC	F2	3.3V/NVCC_CSI	I/O	1403.35	
2	CSI_DATA03	E1	3.3V/NVCC_CSI	I/O	1404.04	
3	CSI_DATA07	D1	3.3V/NVCC_CSI	I/O	1415.99	

4	CSI_DATA01	E3	3.3V/NVCC_CSI	I/O	1418.33	
5	CSI_DATA00	E4	3.3V/NVCC_CSI	I/O	1403.25	
6	CSI_DATA04	D4	3.3V/NVCC_CSI	I/O	1402.85	
7	SD1_CLK	C1	3.3V/1.8V/NVCC_SD	I/O	1141.43	Connect a 10 ohm resistor in series
8	SD1_CMD	C2	3.3V/1.8V/NVCC_SD	I/O	1136.53	Pull-up 10K resistor
9	SD1_DATA2	B1	3.3V/1.8V/NVCC_SD	I/O	1136.12	
10	SD1_DATA3	A2	3.3V/1.8V/NVCC_SD	I/O	1134.1	
11	SD1_DATA1	B2	3.3V/1.8V/NVCC_SD	I/O	1139.39	
12	SD1_DATA0	B3	3.3V/1.8V/NVCC_SD	I/O	1141.27	Pull-up 10K resistor
13	SNVS_TAMPER9	R6	3.3V/SNVS_IN	I/O	1459.22	
14	GPIO1_IO05	M17	3.3V/NVCC_3V3	I/O	2420.05	SD1_VSELECT
15	LCD_ENABLE	B8	3.3V/NVCC_3V3	I/O	1260.39	
16	GPIO1_IO09	M15	3.3V/NVCC_3V3	I/O	1866.4	
17	GPIO1_IO04	M16	3.3V/NVCC_3V3	I/O	2000.23	
18	GPIO1_IO02	L14	3.3V/NVCC_3V3	I/O	1804.53	
19	SNVS_TAMPER2	P11	3.3V/SNVS_IN	I/O	1694.13	
20	SNVS_TAMPER5	N8	3.3V/SNVS_IN	I/O	1797.33	
twenty one	SNVS_TAMPER7	N10	3.3V/SNVS_IN	I/O	1653.61	
twenty two	SNVS_TAMPER8	N9	3.3V/SNVS_IN	I/O	1560.25	
twenty three	BOOT_MODE1	U10	3.3V/SNVS_IN	I/O	1273.49	Pull down 100K on chip
twenty four	BOOT_MODE0	T10	3.3V/SNVS_IN	I/O	1180.99	Pull down 100K on chip
25	SNVS_TAMPER0	R10	3.3V/SNVS_IN	I/O	1420.5	
26	SNVS_TAMPER1	R9	3.3V/SNVS_IN	I/O	1304.59	
27	PWRBTN	R8	3.3V/SNVS_IN	I		Pull-up 100K on chip
28	SNVS_TAMPER4	P9	3.3V/SNVS_IN	I/O	1292.35	
29	VIN_5V		5V/VIN_5V	PWR		
30	VIN_5V		5V/VIN_5V	PWR		

31	DGND		GDN/DGND	PWR		
32	USB_OTG2_VBUS	U12	5V/VBUS_5V	PWR		
33	USB_OTG1_VBUS	T12	5V/VBUS_5V	PWR		
34	USB_OTG2_DP	U13	3.3V/VBUS_3V	I/O	1214.63	
35	USB_OTG2_DN	T13	3.3V/VBUS_3V	I/O	1213.86	
36	USB_OTG1_DP	U15	3.3V/VBUS_3V	I/O	1158.85	
37	USB_OTG1_DN	T15	3.3V/VBUS_3V	I/O	1159.25	
38	USB_OTG1_CHD_B	U16	3.3V/VBUS_3V	I/O		
39	GPIO1_IO00	K13	3.3V/NVCC_3V3	I/O	977.66	
40	UART1_TX_DATA	K14	3.3V/NVCC_3V3	I/O	987.23	
41	GPIO1_IO01	L15	3.3V/NVCC_3V3	I/O	1049.78	
42	UART1_CTS_B	K15	3.3V/NVCC_3V3	I/O	954.91	
43	GPIO1_IO03	L17	3.3V/NVCC_3V3	I/O	945.53	
44	UART1_RX_DATA	K16	3.3V/NVCC_3V3	I/O	889.32	
45	GPIO1_IO07	L16	3.3V/NVCC_3V3	I/O	823.62	
46	GPIO1_IO06	K17	3.3V/NVCC_3V3	I/O	863.33	
47	UART1_RTS_B	J14	3.3V/NVCC_3V3	I/O	888.1	SD1_CD
48	UART2_TX_DATA	J17	3.3V/NVCC_3V3	I/O	817.68	
49	UART2_RX_DATA	J16	3.3V/NVCC_3V3	I/O	823.76	
50	UART2_RTS_B	H14	3.3V/NVCC_3V3	I/O	876.87	
51	UART2_CTS_B	J15	3.3V/NVCC_3V3	I/O	1045.58	
52	UART3_TX_DATA	H17	3.3V/NVCC_3V3	I/O	697.25	
53	UART3_RX_DATA	H16	3.3V/NVCC_3V3	I/O	804.35	
54	UART3_CTS_B	H15	3.3V/NVCC_3V3	I/O	779.01	
55	UART3_RTS_B	G14	3.3V/NVCC_3V3	I/O	863.12	
56	UART4_RX_DATA	G16	3.3V/NVCC_3V3	I/O	845.59	
57	UART4_TX_DATA	G17	3.3V/NVCC_3V3	I/O	862.32	
58	UART5_RX_DATA	G13	3.3V/NVCC_3V3	I/O	997.74	
59	UART5_TX_DATA	F17	3.3V/NVCC_3V3	I/O	873.59	
60	ENET1_RX_ER	D15	3.3V/NVCC_3V3	I/O	922.66	

61	ENET1_TX_CLK	F14	3.3V/NVCC_3V3	I/O	962.62	Connect a 10 ohm resistor in series
62	ENET1_TX_DATA1	E14	3.3V/NVCC_3V3	I/O	956.47	
63	ENET1_TX_EN	F15	3.3V/NVCC_3V3	I/O	953.79	
64	ENET1_RX_DATA0	F16	3.3V/NVCC_3V3	I/O	914.33	
65	ENET1_RX_EN	E16	3.3V/NVCC_3V3	I/O	917.92	
66	ENET1_RX_DATA1	E17	3.3V/NVCC_3V3	I/O	914.14	
67	ENET1_TX_DATA0	E15	3.3V/NVCC_3V3	I/O	956.46	
68	JTAG_MOD	P15	3.3V/NVCC_3V3	I/O	418.19	Pull down 10K resistor
69	JTAG_TRST_B	N14	3.3V/NVCC_3V3	I/O	543.88	
70	JTAG_TMS	P14	3.3V/NVCC_3V3	I/O	496.99	
71	JTAG_TCK	M14	3.3V/NVCC_3V3	I/O	597.6	Pull down 10K resistor
72	JTAG_TDO	N15	3.3V/NVCC_3V3	I/O	581.14	
73	JTAG_TDI	N16	3.3V/NVCC_3V3	I/O	596.89	
74	GPIO1_IO08	N17	3.3V/NVCC_3V3	I/O	507.17	
75	LCD_CLK	A8	3.3V/NVCC_3V3	I/O	1254.77	Connect a 10 ohm resistor in series
76	LCD_HSYNC	D9	3.3V/NVCC_3V3	I/O	1263	
77	LCD_VSYNC	C9	3.3V/NVCC_3V3	I/O	1255.16	
78	VBAT		3.3V/SNVS_IN	PWR		Series diode
79	PWR_ON_EN		3.3V/SNVS_IN	O		
80	RESETN		3.3V/SNVS_IN	I		Pull-up 50K on chip
81	SNVS_TAMPER6	N11	3.3V/SNVS_IN	I/O	1021.68	
82	ENET2_RX_DATA0	C17	3.3V/NVCC_3V3	I/O	844.73	
83	ENET2_RX_DATA1	C16	3.3V/NVCC_3V3	I/O	841.84	
84	ENET2_TX_DATA0	A15	3.3V/NVCC_3V3	I/O	958.69	
85	ENET2_TX_DATA1	A16	3.3V/NVCC_3V3	I/O	955.53	
86	ENET2_RX_ER	D16	3.3V/NVCC_3V3	I/O	847.9	
87	ENET2_RX_EN	B17	3.3V/NVCC_3V3	I/O	839.99	
88	ENET2_TX_EN	B15	3.3V/NVCC_3V3	I/O	953.16	
89	ENET2_TX_CLK	D17	3.3V/NVCC_3V3	I/O	961.17	Connect a 10 ohm resistor in series
90	DGND		GDN/DGND	PWR		
91	LCD_DATA23	B16	3.3V/NVCC_3V3	I/O	1256.56	Pull down 47K resistor

92	LCD_DATA22	A14	3.3V/NVCC_3V3	I/O	1255.86	Pull down 47K resistor
93	LCD_DATA21	B14	3.3V/NVCC_3V3	I/O	1253.74	Pull down 47K resistor
94	LCD_DATA20	C14	3.3V/NVCC_3V3	I/O	1254.8	Pull down 47K resistor
95	LCD_DATA19	D14	3.3V/NVCC_3V3	I/O	1259.93	Pull down 47K resistor
96	LCD_DATA18	A13	3.3V/NVCC_3V3	I/O	1258.43	Pull down 47K resistor
97	LCD_DATA17	B13	3.3V/NVCC_3V3	I/O	1262.46	Pull down 47K resistor
98	LCD_DATA16	C13	3.3V/NVCC_3V3	I/O	1258.38	Pull down 47K resistor
99	LCD_DATA15	D13	3.3V/NVCC_3V3	I/O	1258.67	Pull down 47K resistor
100	LCD_DATA14	A12	3.3V/NVCC_3V3	I/O	1264.02	Pull down 47K resistor
101	LCD_DATA13	B12	3.3V/NVCC_3V3	I/O	1254.09	Pull down 47K resistor
102	LCD_DATA12	C12	3.3V/NVCC_3V3	I/O	1260.01	Pull down 47K resistor
103	LCD_DATA11	D12	3.3V/NVCC_3V3	I/O	1259.66	Pull down 47K resistor
104	LCD_DATA10	E12	3.3V/NVCC_3V3	I/O	1263.43	Pull down 47K resistor
105	LCD_DATA09	A11	3.3V/NVCC_3V3	I/O	1266.07	Pull down 47K resistor
106	LCD_DATA08	B11	3.3V/NVCC_3V3	I/O	1262.66	Pull down 47K resistor
107	LCD_DATA07	D11	3.3V/NVCC_3V3	I/O	1265.28	Pull down 47K resistor
108	LCD_DATA06	A10	3.3V/NVCC_3V3	I/O	1263.9	Pull down 47K resistor
109	LCD_DATA05	B10	3.3V/NVCC_3V3	I/O	1258.33	Pull down 47K resistor
110	LCD_DATA04	C10	3.3V/NVCC_3V3	I/O	1262.71	Pull down 47K resistor
111	LCD_DATA03	D10	3.3V/NVCC_3V3	I/O	1267.14	Pull down 47K resistor
112	LCD_DATA02	E10	3.3V/NVCC_3V3	I/O	1263.66	Pull down 47K resistor
113	LCD_DATA01	A9	3.3V/NVCC_3V3	I/O	1266.95	Pull down 47K resistor
114	LCD_DATA00	B9	3.3V/NVCC_3V3	I/O	1267.01	Pull down 47K resistor
115	CSI_DATA05	D3	3.3V/NVCC_CSI	I/O	1406.5	
116	CSI_PIXCLK	E5	3.3V/NVCC_CSI	I/O	1405.97	
117	CSI_DATA06	D2	3.3V/NVCC_CSI	I/O	1403.32	
118	CSI_DATA02	E2	3.3V/NVCC_CSI	I/O	1403.22	
119	CSI_MCLK	F5	3.3V/NVCC_CSI	I/O	1412.79	
120	CSI_HSYNC	F3	3.3V/NVCC_CSI	I/O	1405.65	

Note: The unit of trace length is mil.

4.3.2. I/O impedance control

Generally, the single-ended signal impedance is controlled at 50 ohms, and the differential signal impedance is controlled as shown in the following table.

Differential trace impedance control table

Pinout	Pin Name	Trace length	Impedance Control	illustrate
36/37	USB_OTG1_DP / USB_OTG1_DN	1158.85/1159.25	90 ohm	USB Signal
34/35	USB_OTG2_DP / USB_OTG2_DN P	1214.63/1213.86	90 ohm	USB Signal

4.4.Electrical characteristics

4.4.1. Power consumption

Note: The following parameters are measured on the ECK20-6Y28A5ME8G-I core board at room temperature. The measured power consumption does not include the baseboard power consumption. There is no display when measuring heavy-load power consumption, no baseboard SDIO access, and no network access.

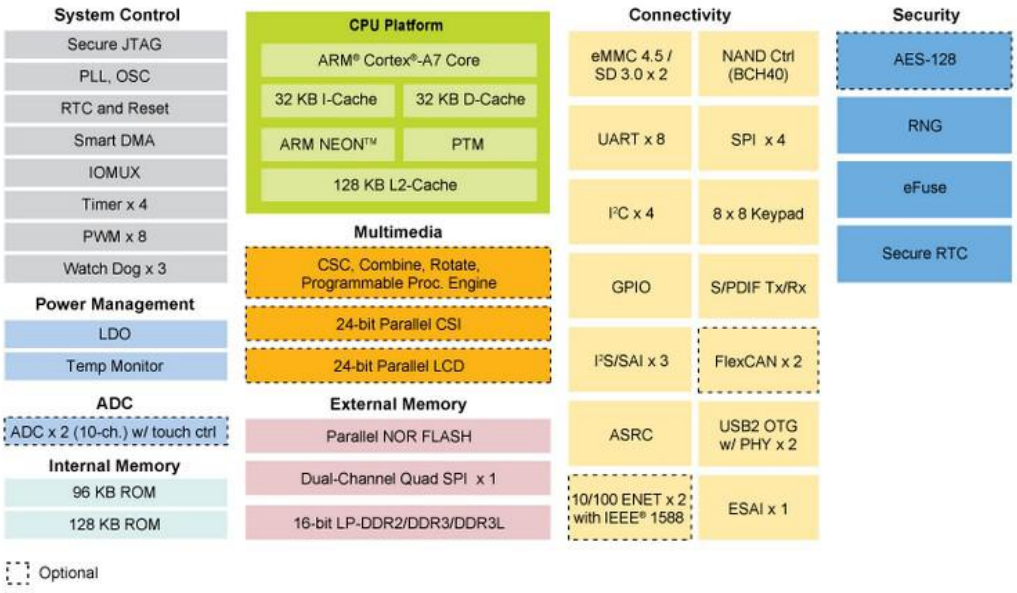
Power Consumption Table

Power Status	Test environment	Supply voltage	Current	Power consumption
PWRUP	After the system starts, no application is running	5.0V	0.075A	0.375W
PWRUP	Software reload testing	5.0V	0.220A	1.1W
SLEEP	Freeze mode hibernation	5.0V	0.042A	0.21W
SLEEP	Standby mode sleep state	5.0V	0.011A	0.055W
SLEEP	mem mode sleep state	5.0V	0.003A	0.015W
PWRDN	Power off state power consumption	5.0V	0.00A	0W

5. Core Board Hardware Design

5.1.Processor

The ECK20-6Y2XA series core board uses the MCIMX6Y2CVM08AB processor from the i.MX6ULL series. The i.MX6ULL series is a low-power, high-performance, and low-cost application processor based on the ARM Cortex A7 core. Compared with the i.MX6UL series, the i.MX6ULL series has simplified some encryption functions while maintaining high cost-effectiveness and ultra-low power. It can be regarded as a cost-optimized version of the i.MX6UL series. The functional block diagram of the i.MX6ULL series is shown below.



i.MX6ULL Series Functional Block Diagram

The main features of the MCIMX6Y2CVM08AB processor are as follows:

- ARM® Cortex®-A7 core, running at 792MHz;
- 16-bit LP-DDR2, DDR3/DDR3L memory interface;
- 8-bit parallel NAND FLASH interface;
- 16/8-bit parallel NOR FLASH interface;
- Parallel LCD display with resolution up to WXGA (1366x768);
- 24/16/10/8-bit parallel camera sensor interface;
- Two CAN interfaces;
- A Quad SPI NOR FLASH interface;
- Two USB 2.0 OTG ports;
- Two 10/100 Ethernet ports, supporting IEEE 1588 protocol;
- Two MMC 4.5/SD 3.0/SDIO ports;
- Audio interfaces include 3 I2S/SAI, S/PDIF Tx/Rx;
- Eight UART interfaces;
- Two ADC modules, supporting up to 10 input channels.

5.2.Memory

The ECK20-6Y2XA series core board has a DDR3L SDRAM memory chip mounted on t

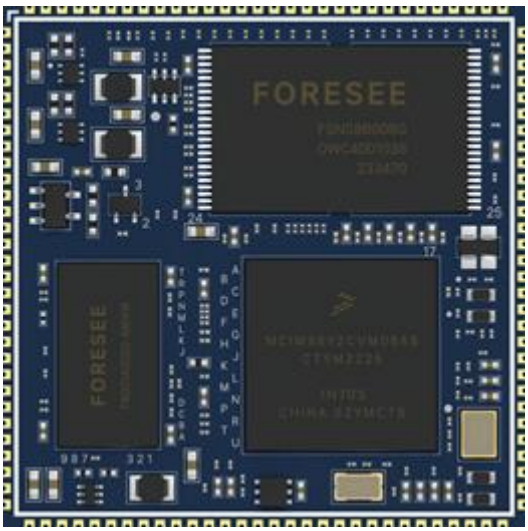
he board. It is designed with a 16-bit memory data width and has two optional capacities: 256 MB/512MB.

5.3.Clock

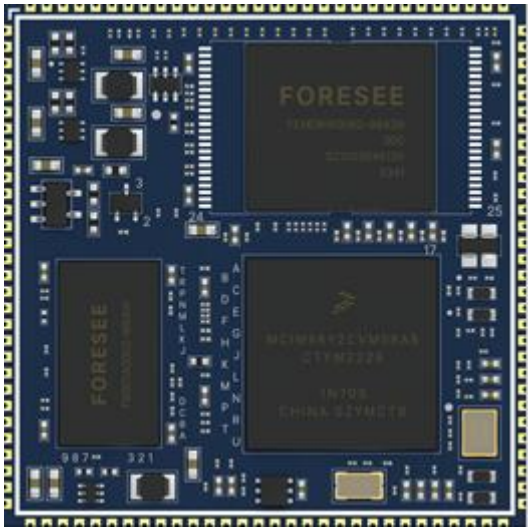
The ECK20-6Y2XA series core board provides one 32.768KHz crystal (passive) oscillator circuit and one 24MHz crystal (passive) oscillator circuit on the board as the processor system clock source.

5.4.Storage

The ECK20-6Y2XA series core board has two storage solutions designed on the board. One is the parallel FLASH storage solution. This storage solution uses SLC NAND FLASH chips as storage media, which has the characteristics of low cost and high reliability. The other is the eMMC storage solution. This storage solution uses eMMC chips as storage media, which has the characteristics of large storage capacity, low unit storage cost and easy use. Because the two storage solutions reuse the same I/O resources, a core board product of one model only supports one storage solution. Users need to select the corresponding model of core board products according to the storage requirements of specific projects. The physical pictures of the two storage solutions are shown in the figure below.



NAND FLASH storage solution products



eMMC Storage Solution Products

The eMMC memory is connected to the USDHC2 functional interface and shares the I/O pins with the NAND interface. The signal level of the eMMC chip and processor interface onl y supports 3.3V level, not 1.8V level, so the USDHC2 interface only supports a maximum clo ck frequency of 50MHz. The software should pay attention to the parameter configuration of USDHC2.

5.4.1. Multiplexed I/O allocation

Storage I/O Allocation Table

MPU I/O Pins	NAND Features	eMMC Features
D7	NAND_DATA0	eMMC_DATA0
B7	NAND_DATA1	eMMC_DATA1
A7	NAND_DATA2	eMMC_DATA2
D6	NAND_DATA3	eMMC_DATA3
C6	NAND_DATA4	eMMC_DATA4
B6	NAND_DATA5	eMMC_DATA5
A6	NAND_DATA6	eMMC_DATA6
A5	NAND_DATA7	eMMC_DATA7
A3	NAND_nREADY	
D8	NAND_nRE	eMMC_CLK
C5	NAND_nCE0	
B5	NAND_nCE1	
A4	NAND_CLE	
B4	NAND_ALE	eMMC_RST#
C8	NAND_nWE	eMMC_CMD
D5	NAND_nWP	
E6	NAND_DQS	

5.5.Watchdog

The ECK20-6Y2XA series core board supports 1 watchdog function. The watchdog timeout output can generate a low level pulse (about 1.6ms wide) on the RESETN signal pin and cause a system reset.

5.6.Power supply

The ECK20-6Y2XA series core board adopts a separate power supply solution, which is designed strictly in accordance with the voltage, power and timing requirements in the i.MX6ULL manual. The ECK20-6Y2XA series core board power supply solution supports automatic adjustment of the SD1 I/O interface voltage, and automatically selects 3.3V or 1.8VI/O supply voltage according to the SDIO rate requirements. The ECK20-6Y2XA series core board power supply solution does not support the dynamic adjustment function of the CPU core power voltage.

5.6.1. Power domain

The ECK20-6Y2XA series core board is powered by a single DC +5V power supply. Only one VIN_5V power input is needed externally. Other power supplies are generated internally by the core board, and no additional power supply is required. The power domains and typical voltages to which the power rails belong are shown in the following table. The SNVS power domain is powered on first, the NVCC power domain is powered on after the SNVS power domain, and the VBUS power domain can be powered on at any time. When using the core board, pay attention to the power domain to which the signal belongs and the power-on order of each power domain.

Power Domain Table

Power supply name	Power Description	Typical voltage	Power Domain
VIN_5V	Core board 5V main power input	5.0V	SNVS
SNVS_IN	SNVS Power Rail	3.3V	SNVS
NVCC_3V3/CSI	I/O interface power rail	3.3V	NVCC
NVCC_SD	SDIO interface power rail	1.8V/3.3V	NVCC
VBUS_5V	USB interface 5V power rail	5.0V	VBUS
VBUS_3V	USB interface 3V power rail	3.3V	VBUS

5.6.2. Multiplexed I/O allocation

Power I/O Assignment Table

MPU I/O Pins	Network Name	Function
T9	SNVS_PMIC_ON_REQ	Processor power management output
M17	GPIO1_IO05	SD1 I/O voltage adjustment

6. Baseboard Hardware Design

6.1.Power interface

For embedded product design, the design of the power supply system is crucial. It not only needs to consider the basic electrical parameters of the power supply itself, but also the stability design, timing design and other factors of the power supply. The ECK20-6Y2XA series core board adopts a single power supply solution and provides power timing management signals to simplify the user's baseboard power supply design as much as possible.

6.1.1. Power input

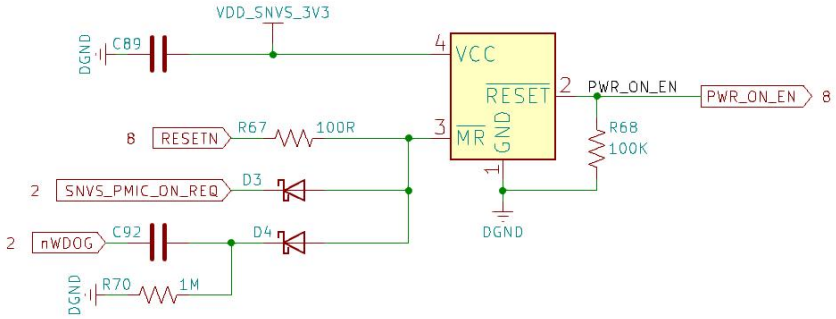
The ECK20-6Y2XA series core board is powered by a single DC +5V power supply, corresponding to pins 29 and 30 of the stamp hole connector. The power supply voltage range is 5.0V±10%. The normal power consumption of the ECK20-6Y2XA series core board is about 1 W. When designing the power supply for the core board, the baseboard should consider the increase in power consumption when I/O and more functions are running at the same time, and the increase in power consumption of components at high temperature. Therefore, it is recommended that the core board power supply current be designed to be about 0.5A.

If a DC-DC power supply is used to power the core board, the power margin should not be too large when designing the power supply. If the power design is too large, many power supplies will work in discontinuous PWM mode to ensure conversion efficiency, and the output power ripple will increase significantly, which is not conducive to the working stability of the digital signal system. If an LDO is used to power the core board, the power loss and operating temperature rise of the LDO itself should be considered during design to prevent the LD

O power supply from overheating and stopping working or burning when working in a high te mperature environment or an environment with poor heat dissipation.

6.1.2. Power control

The ECK20-6Y2XA series core board outputs a power management control signal PWR_O N_EN. When this signal is valid (high level), it indicates that the NVCC power domain power is enabled. The user baseboard can use this signal to control the power supply of the relevan t power domain of the baseboard to start working. The PWR_ON_EN signal is invalid when t he manual reset is valid (low level), or the SNVS_PMIC_ON_REQ signal is invalid (low leve l), or the watchdog timeout signal is valid (low level). The PWR_ON_EN generation circuit is shown in the figure below.



PWR_ON_EN generation circuit

Note: Reset (this product reset is designed as a cold reset, which will cause part of the p ower supply to shut down) and power on/off operations will cause the power system to lose p ower partially or completely. Due to the presence of capacitors or circuit design requirements, the power supply of some circuits cannot be quickly reduced to 0V and needs a period of tim e to discharge. If you reset or switch the power on and off multiple times in a short period o f time, some I/O interfaces or chips may be powered on abnormally, causing failure to start or more serious failures. It is recommended that the interval between reset or power on/off be g reater than 2-3 seconds.

When designing the baseboard power supply, attention should be paid to the power rail, working level, power-on timing and other characteristics of the I/O signal. The pin definition t able in this manual describes in detail the level, power rail and other characteristics of the cor e board I/O interface. When the core board I/O signal is connected to the baseboard chip, it i s necessary to determine whether the chip pin and the core board I/O are at the same level, t

he same power rail or power-on time domain. Connecting two I/O signals with wrong levels o r power-on time domains together may cause communication failures, reduce the life of the I/ O interface, or damage the I/O interface. For example, when designing the CAN interface, so me development board products on the market connect the core board 3.3V I/O signal to the CAN interface chip powered by a 5V power supply (core board power supply). There are two problems with this design. One is that the core board 3.3V I/O signal may not tolerate the 5 V signal of the CAN interface chip, resulting in unstable communication or I/O damage; the o ther is that the 5V power supply is powered on before the 3.3V I/O, and they are not in the same time domain. When 3.3V is not powered on after 5V is powered on, the 5V power supp ly will enter the 3.3V power supply network through the I/O connection, causing the voltage o f the 3.3V power supply network to increase, which may cause abnormal startup of some devi ces or damage to the I/O interface.

6.1.3. Backup power

VBAT is the backup battery interface, corresponding to pin 78 of the stamp hole connecto r, and can be powered by an external RTC battery. Its function is to supply power to the core board SNVS power domain through an external battery when the core board 5V power suppl y is powered off, which can maintain the normal operation of the processor's internal RTC fun ction, power management function, and some configuration registers. The voltage range of VB AT is 2.6-3.3V. A diode is connected in series between the VBAT backup battery interface and the processor VDD_SNVS_IN pin. If VBAT is powered by an external battery, the bottom bo ard does not need to be connected in series with a diode.

After the processor is powered off, the SNVS power domain consumes a lot of power. If an external RTC battery is used for power supply, the RTC battery life will be too short. NX P recommends using an external RTC circuit to implement the RTC function. If an external R TC circuit is used, the VBAT pin can be left floating.

6.1.4. Pin definition

Power pin definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
29	VIN_5V		5V/VIN_5V	PWR		
30	VIN_5V		5V/VIN_5V	PWR		

78	VBAT		3.3V/SNVS_IN	PWR		Series diode
79	PWR_ON_EN		3.3V/SNVS_IN	O		

6.2.Launch configuration

i. When the MX6ULL processor starts up, it will first execute the program in the Boot ROM inside the chip. The Boot ROM will determine the boot mode and boot device based on the status of the BOOT_MODE register, eFUSEs, configuration pins, etc.

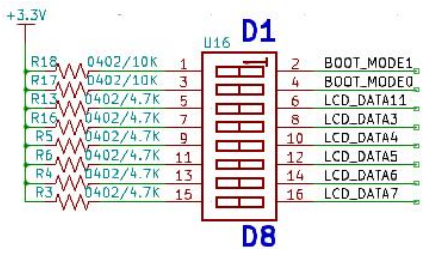
The value of the BOOT_MODE register depends on the levels of the two pins BOOT_MODE0 and BOOT_MODE1 in the initial power-on phase, which determines the boot mode. The specific corresponding relationship is as follows:

BOOT_MODE boot mode configuration table

BOOT_MODE[1:0]	Startup Mode	Startup Mode Description
00	Boot From Fuses	Read the startup information from the internal fuses. This method is recommended for mass production.
01	Serial Downloader	Supports downloading programs to Flash from USB_OTG1 port. It should be noted that in this mode, UART1 and UART2 have higher priority than USB_OTG. If UART1 and UART2 serial ports detect data in this mode, the downloader cannot burn the program from USB and the computer cannot detect the device.
10	Internal Boot	Read the startup configuration from the Boot Mode pin. This is recommended for development mode and can also be used for mass production.
11	Reserved	Retention mode.

Usually, the BOOT mode is set to internal Boot mode. In this mode, the CPU will read the level status of LCD_DATA0-DATA23 pins to determine the boot device when it is powered on and reset. LCD_DATA0-DATA23 has been pulled down internally by the ECK20-6Y2XA series core board. When designing the baseboard, only individual pins need to be configured. The baseboard BOOT device selection configuration reference circuit is shown in the figure below.

SW								
D1	D2	D3	D4	D5	D6	D7	D8	BOOT DEVICE
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	USB
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	MicroSD
ON	OFF	ON	OFF	OFF	ON	ON	OFF	EMMC
ON	OFF	OFF	OFF	ON	OFF	OFF	ON	NAND



BOOT configuration circuit

LCD_DATA0-DATA7 pins correspond to BOOT configuration function BOOT_CFG1[0]-CFG1[7]. LCD_DATA8-DATA15 pins correspond to BOOT configuration function BOOT_CFG2[0]-CFG2[7]. LCD_DATA16-DATA23 pins correspond to BOOT configuration function BOOT_CFG4[0]-CFG4[7]. The BOOT_CFG configuration function is shown in the figure below.

	0/1	0/1	0/1	1	0	0	0	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Selfor SDR50 and SDR104 only '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Selfor SDR50 and SDR104 only '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

BOOT_CFG1 Configuration Diagram

	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0 : one clock delay 1: two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

BOOT_CFG2 Configuration Diagram

	0	0	0	0	0	0	0	0
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT MMU _DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC IOMUX SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_DE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

BOOT_CFG4 configuration diagram

6.2.1. Pin definition

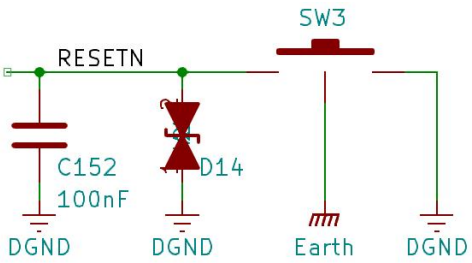
Startup configuration pin definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
twenty three	BOOT_MODE1	U10	3.3V/SNVS_IN	I	1273.49	Pull down 100K on chip
twenty four	BOOT_MODE0	T10	3.3V/SNVS_IN	I	1180.99	Pull down 100K on chip
107	LCD_DATA07	D11	3.3V/NVCC_3V3	I/O	1265.28	Pull down 47K resistor
108	LCD_DATA06	A10	3.3V/NVCC_3V3	I/O	1263.9	Pull down 47K resistor
109	LCD_DATA05	B10	3.3V/NVCC_3V3	I/O	1258.33	Pull down 47K resistor
110	LCD_DATA04	C10	3.3V/NVCC_3V3	I/O	1262.71	Pull down 47K resistor
111	LCD_DATA03	D10	3.3V/NVCC_3V3	I/O	1267.14	Pull down 47K resistor
103	LCD_DATA11	D12	3.3V/NVCC_3V3	I/O	1259.66	Pull down 47K resistor

6.3.Reset and power buttons

the ECK20-6Y2XA series core board can be connected to external buttons to achieve proc essor reset and power control.

The RESETN signal is designed with a de-jitter circuit and a pull-up resistor in the core board. The PWRBTN signal is connected to the processor chip ONOFF pin in the core board, and the processor chip has a pull-up resistor. Since these two signals have pull-up resistors in the core board, do not connect the pull-up resistors when using the baseboard. Connect the b uttons directly or drive through the OD gate. The reference schematic diagram of the buttons i s shown in the figure below.



Button reference schematic

Note: Do not pull up the reset and power button signals through resistors at will. If the p ull-up power rail is incorrect, it will cause uncertain signals to be input to the button signal in terface when the system is in standby or shut down. For example, some baseboard designs pul l up the PWRBTN signal to the NVCC_3V3 power supply. When the system is shut down, th e NVCC_3V3 power supply is also turned off. At this time, the NVCC_3V3 power supply vol tage drops to 0V, and the PWRBTN signal pulls up the NVCC_3V3 power supply and becom

es pulled down to the ground, which is equivalent to pressing the PWRBTN button and the sy stem restarts, which eventually causes the system to fail to shut down normally through softwa re.

6.3.1. Pin definition

Button pin definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
27	PWRBTN	R8	3.3V/SNVS_IN	I		Pull-up 100K on chip
80	RESETN		3.3V/SNVS_IN	I		Pull-up 50K on chip

6.4.Display interface

The ECK20-6Y2XA series core board provides a parallel LCD display interface with a ma ximum resolution of 1366 x 768@60fps and a maximum pixel clock of 85MHz. It supports 2 4/18/16/8-bit parallel display. Customers can configure the display resolution and display data f ormat according to their needs. In LCD and TFT screen applications, GPIO can be used to co ntrol the screen power and backlight power. PWM output can be used to control the backlight brightness. You can also use I2C and GPIO external interrupt functions to connect the touch screen. You can choose to use Ebyte's LCD touch screen module. For detailed module informa tion, please refer to the official website https://www.ebyte.com/.

6.4.1. Interface definition

Display interface definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
15	LCD_ENABLE	B8	3.3V/NVCC_3V3	I/O	1260.39	
75	LCD_CLK	A8	3.3V/NVCC_3V3	I/O	1254.77	Connect a 10 ohm resistor in series
76	LCD_HSYNC	D9	3.3V/NVCC_3V3	I/O	1263	
77	LCD_VSYNC	C9	3.3V/NVCC_3V3	I/O	1255.16	
91	LCD_DATA23	B16	3.3V/NVCC_3V3	I/O	1256.56	Pull down 47K resistor
92	LCD_DATA22	A14	3.3V/NVCC_3V3	I/O	1255.86	Pull down 47K resistor
93	LCD_DATA21	B14	3.3V/NVCC_3V3	I/O	1253.74	Pull down 47K resistor
94	LCD_DATA20	C14	3.3V/NVCC_3V3	I/O	1254.8	Pull down 47K resistor
95	LCD_DATA19	D14	3.3V/NVCC_3V3	I/O	1259.93	Pull down 47K resistor
96	LCD_DATA18	A13	3.3V/NVCC_3V3	I/O	1258.43	Pull down 47K resistor
97	LCD_DATA17	B13	3.3V/NVCC_3V3	I/O	1262.46	Pull down 47K resistor
98	LCD_DATA16	C13	3.3V/NVCC_3V3	I/O	1258.38	Pull down 47K resistor

99	LCD_DATA15	D13	3.3V/NVCC_3V3	I/O	1258.67	Pull down 47K resistor
100	LCD_DATA14	A12	3.3V/NVCC_3V3	I/O	1264.02	Pull down 47K resistor
101	LCD_DATA13	B12	3.3V/NVCC_3V3	I/O	1254.09	Pull down 47K resistor
102	LCD_DATA12	C12	3.3V/NVCC_3V3	I/O	1260.01	Pull down 47K resistor
103	LCD_DATA11	D12	3.3V/NVCC_3V3	I/O	1259.66	Pull down 47K resistor
104	LCD_DATA10	E12	3.3V/NVCC_3V3	I/O	1263.43	Pull down 47K resistor
105	LCD_DATA09	A11	3.3V/NVCC_3V3	I/O	1266.07	Pull down 47K resistor
106	LCD_DATA08	B11	3.3V/NVCC_3V3	I/O	1262.66	Pull down 47K resistor
107	LCD_DATA07	D11	3.3V/NVCC_3V3	I/O	1265.28	Pull down 47K resistor
108	LCD_DATA06	A10	3.3V/NVCC_3V3	I/O	1263.9	Pull down 47K resistor
109	LCD_DATA05	B10	3.3V/NVCC_3V3	I/O	1258.33	Pull down 47K resistor
110	LCD_DATA04	C10	3.3V/NVCC_3V3	I/O	1262.71	Pull down 47K resistor
111	LCD_DATA03	D10	3.3V/NVCC_3V3	I/O	1267.14	Pull down 47K resistor
112	LCD_DATA02	E10	3.3V/NVCC_3V3	I/O	1263.66	Pull down 47K resistor
113	LCD_DATA01	A9	3.3V/NVCC_3V3	I/O	1266.95	Pull down 47K resistor
114	LCD_DATA00	B9	3.3V/NVCC_3V3	I/O	1267.01	Pull down 47K resistor

6.4.2. Layout suggestions

- ❖If the LCD signal of the baseboard is designed with a series matching resistor, it is recommended to place it close to the stamp hole of the core board;
- ❖The LCD signal has been processed into equal length in the core board. The length of the wiring in the core board can be found in the pin definition table;
- ❖The LCD signal in the core board is controlled according to the single-ended 50Ω ±10% impedance, and the impedance control of the baseboard is recommended to be consistent;
- ❖It is recommended that the baseboard LCD signal lines be of equal length, with an error range of ±100mil and a signal line spacing of at least 2W.

6.5.Camera interface

of the ECK20-6Y2XA series core board supports 8-bit or 24-bit YCbCr, YUV, RGB format data input; 8-bit, 10-bit or 16-bit Bayer format data input, and the maximum pixel clock is 133.3MHz. The camera interface will occupy a large number of I/O pins in the application, reducing other multiplexing functions. It is recommended to use a USB interface camera to realize the camera function.

6.5.1. Interface definition

Camera interface definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
119	CSI_MCLK	F5	3.3V/NVCC_CSI	I/O	1412.79	CSI Master Clock
116	CSI_PIXCLK	E5	3.3V/NVCC_CSI	I/O	1405.97	CSI Pixel Clock
1	CSI_VSYNC	F2	3.3V/NVCC_CSI	I/O	1403.35	CSI vertical synchronization signal
120	CSI_HSYNC	F3	3.3V/NVCC_CSI	I/O	1405.65	CSI horizontal synchronization signal
5	CSI_DATA00	E4	3.3V/NVCC_CSI	I/O	1403.25	CSI data bits
4	CSI_DATA01	E3	3.3V/NVCC_CSI	I/O	1418.33	CSI data bits
118	CSI_DATA02	E2	3.3V/NVCC_CSI	I/O	1403.22	CSI data bits
2	CSI_DATA03	E1	3.3V/NVCC_CSI	I/O	1404.04	CSI data bits
6	CSI_DATA04	D4	3.3V/NVCC_CSI	I/O	1402.85	CSI data bits
115	CSI_DATA05	D3	3.3V/NVCC_CSI	I/O	1406.5	CSI data bits
117	CSI_DATA06	D2	3.3V/NVCC_CSI	I/O	1403.32	CSI data bits
3	CSI_DATA07	D1	3.3V/NVCC_CSI	I/O	1415.99	CSI data bits

6.6.uSDHC card interface

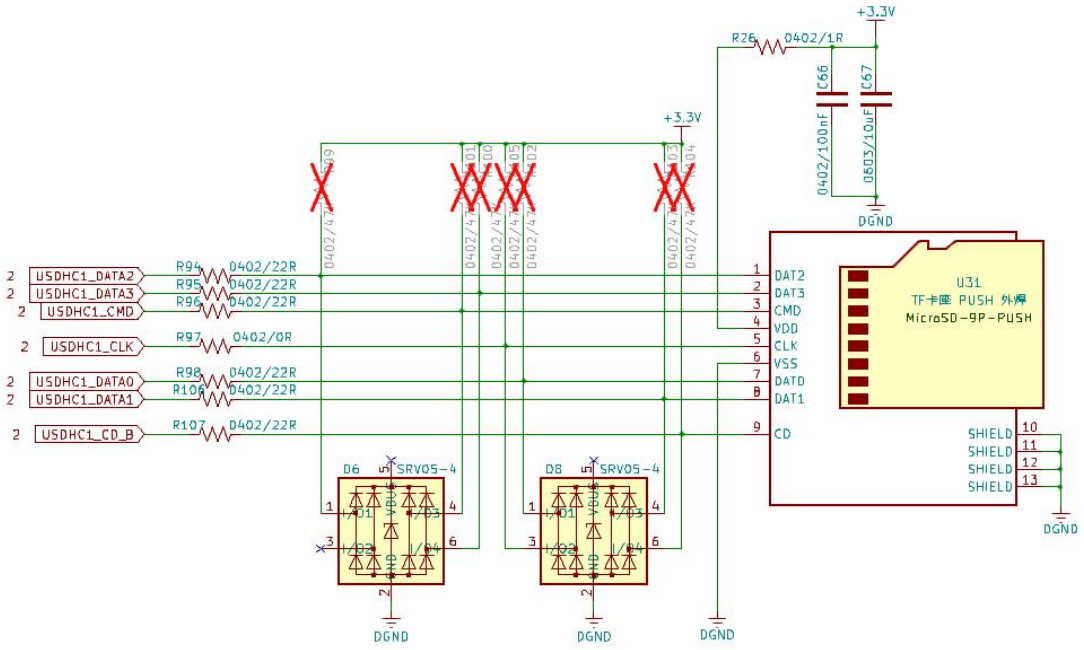
The ECK20-6Y2XA series core board is equipped with 2 uSDHC interfaces. The uSDHC interface (Ultra Secured Digital Host Controller) is a unique secure digital host interface of N XP, which provides a secure communication method between the processor and external SD/SD IO/MMC interface devices.

The uSDHC 1 function of the processor is externally led out and can be used for SD car d startup or SDIO communication. uSDHC 2 is only externally led out through I/O multiplexin g on the core board using the NAND FLASH storage solution. On the core board using the e MMC storage solution, the uSDHC 2 function is occupied and cannot be led out.

of the ECK20-6Y2XA series core board can support automatic adjustment of I/O power s upply. The I/O level of the uSDHC 1 interface is adjusted through GPIO1_IO05, and can supp ort 3.3V and 1.8V levels. At 1.8V level, the uSDHC 1 interface supports a maximum clock fr equency of 150MHz.

The processor's I/O can be configured with on-chip pull-up resistors. These pull-up resistor s can meet the pull-up requirements when the SD card interface is expanded, and the user des ign does not need external pull-up resistors. The core board has already connected a 10 ohm

matching resistor in series with the uSDHC clock signal, and the user design does not need e xternal series resistors. To expand the Micro SD card through the uSDHC interface, you can r efer to the following schematic design.



SD card reference circuit diagram

6.6.1. Pin definition

uSDHC interface signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
7	SD1_CLK	C1	3.3V/1.8V/NVCC_SD	I/O	1141.43	Connect a 10 ohm resistor in series
8	SD1_CMD	C2	3.3V/1.8V/NVCC_SD	I/O	1136.53	Pull-up 10K resistor
9	SD1_DATA2	B1	3.3V/1.8V/NVCC_SD	I/O	1136.12	
10	SD1_DATA3	A2	3.3V/1.8V/NVCC_SD	I/O	1134.1	
11	SD1_DATA1	B2	3.3V/1.8V/NVCC_SD	I/O	1139.39	
12	SD1_DATA0	B3	3.3V/1.8V/NVCC_SD	I/O	1141.27	Pull-up 10K resistor
14	GPIO1_IO05	M17	3.3V/NVCC_3V3	I/O	2420.05	SD1_VSELECT
47	UART1_RTS_B	J14	3.3V/NVCC_3V3	I/O	888.1	SD1_CD

6.6.2. Layout suggestions

- The uSDHC signal in the core board is controlled according to the single-ended 50Ω ± 10% impedance, and the impedance control of the baseboard is recommended to be consistent;

- ❖The uSDHC signal has been processed into equal length in the core board. The length of the trace in the core board can be found in the pin definition table;
- ❖It is recommended that the uSDHC signal (excluding the insertion detection signal) of the baseboard be routed with equal length control, with an error range of ±100mil and a signal line spacing of at least 2W.
- ❖The distance between the clock signal and other signals follows the 3W rule.

6.7.USB interface

The ECK20-6Y2XA series core board supports 2 USB 2.0 OTG interfaces. If the user uses the USB OTG function, the USB interface is recommended to use the MICRO USB interface, because the interface is a 5-wire interface with USB_ID (which can be realized through GPIO function multiplexing) signal, which can be used to identify the HOST and DEVICE, thereby realizing the OTG function. If the user does not use the USB OTG function and only uses it as a USB HOST, then the USB interface can choose a 4-wire or 5-wire interface.

USB_OTGx_VBUS is the power supply for the USB interface I/O of the processor. To use the USB function, the USB interface I/O needs to be powered through these two pins, with a supply voltage of 5.0V±10% and a maximum supply current of 50mA.

6.7.1. Pin definition

USB interface signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
32	USB_OTG2_VBUS	U12	5V/VBUS_5V	PWR		VBUS power input
33	USB_OTG1_VBUS	T12	5V/VBUS_5V	PWR		VBUS power input
34	USB_OTG2_DP	U13	3.3V/VBUS_3V	I/O	1214.63	
35	USB_OTG2_DN	T13	3.3V/VBUS_3V	I/O	1213.86	
36	USB_OTG1_DP	U15	3.3V/VBUS_3V	I/O	1158.85	
37	USB_OTG1_DN	T15	3.3V/VBUS_3V	I/O	1159.25	
38	USB_OTG1_CHD_B	U16	3.3V/VBUS_3V	I/O		

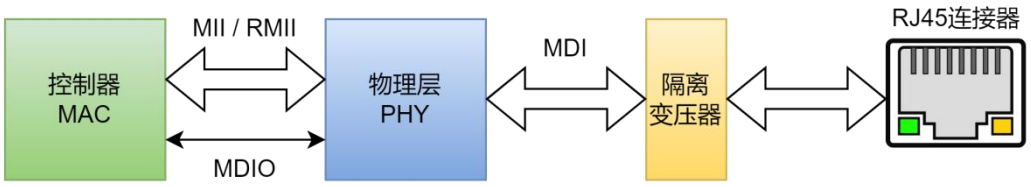
6.7.2. Layout suggestions

- ❖The USB signal routing is controlled to be of equal length;
- ❖The differential impedance of the USB signal is controlled at 90Ω;
- ❖Keep the USB signal cable as short as possible.

6.8.Ethernet interface

The ECK20-6Y2XA series core board supports 2-way 10M/100M Ethernet controller. The Ethernet controller supports RMII and MII interfaces. The number of signal lines of the RMII interface is reduced by half compared to the MII interface, which can simplify the design and save resources. Therefore, the core board is recommended to use the RMII interface to connect to the Ethernet PHY.

Usually an RJ45 Ethernet interface is mainly composed of an Ethernet controller MAC (Media Access Control), an Ethernet physical layer interface PHY (Physical Layer), an Ethernet transformer, and an RJ45 connector, as shown in the figure below.



RJ45 Ethernet components

The ECK20-6Y2XA series core board does not have an Ethernet PHY circuit designed in it. If the user uses the Ethernet function, the PHY interface chip circuit needs to be designed on the baseboard. The baseboard PHY interface chip circuit design can refer to the Ebyte i.MX6ULL single-board computer product drawing.

6.8.1. Pin definition

Ethernet interface signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
60	ENET1_RX_ER	D15	3.3V/NVCC_3V3	I/O	922.66	RMII Signals
61	ENET1_TX_CLK	F14	3.3V/NVCC_3V3	I/O	962.62	RMII signal, connect 10 ohm resistor in series
62	ENET1_TX_DATA1	E14	3.3V/NVCC_3V3	I/O	956.47	RMII Signals
63	ENET1_TX_EN	F15	3.3V/NVCC_3V3	I/O	953.79	RMII Signals
64	ENET1_RX_DATA0	F16	3.3V/NVCC_3V3	I/O	914.33	RMII Signals
65	ENET1_RX_EN	E16	3.3V/NVCC_3V3	I/O	917.92	RMII Signals
66	ENET1_RX_DATA1	E17	3.3V/NVCC_3V3	I/O	914.14	RMII Signals
67	ENET1_TX_DATA0	E15	3.3V/NVCC_3V3	I/O	956.46	RMII Signals
82	ENET2_RX_DATA0	C17	3.3V/NVCC_3V3	I/O	844.73	RMII Signals
83	ENET2_RX_DATA1	C16	3.3V/NVCC_3V3	I/O	841.84	RMII Signals
84	ENET2_TX_DATA0	A15	3.3V/NVCC_3V3	I/O	958.69	RMII Signals

85	ENET2_TX_DATA1	A16	3.3V/NVCC_3V3	I/O	955.53	RMII Signals
86	ENET2_RX_ER	D16	3.3V/NVCC_3V3	I/O	847.9	RMII Signals
87	ENET2_RX_EN	B17	3.3V/NVCC_3V3	I/O	839.99	RMII Signals
88	ENET2_TX_EN	B15	3.3V/NVCC_3V3	I/O	953.16	RMII Signals
89	ENET2_TX_CLK	D17	3.3V/NVCC_3V3	I/O	961.17	RMII signal, connect 10 ohm resistor in series
45	GPIO1_IO07	L16	3.3V/NVCC_3V3	I/O	823.62	ENET_MDC
46	GPIO1_IO06	K17	3.3V/NVCC_3V3	I/O	863.33	ENET_MDIO

6.8.2. Layout suggestions

- ❖RMII signal is used for equal length control, with an error of ±100mil and a line spacing of more than 2W;
- ❖The network differential signal is controlled to be equal length, the error within the differential pair is ±30mil, and the spacing between adjacent differential pairs is more than 3W;
- ❖The network port transformer should be placed close to the PHY chip, and the recommended distance is no more than 20 mm.
- ❖The decoupling capacitor of the power pin of the PHY chip is placed close to the PHY chip;

6.9.Audio interface

The ECK20-6Y2XA core board supports up to 3 synchronous audio interfaces (SAI), which supports full-duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM and codec/DSP interfaces. In the backplane circuit design, the SAI interface signal needs to be connected to the audio codec chip to realize the audio interface functions such as headphones, microphones, speakers, etc. through the audio codec chip .

The AUDIO_GND in the audio circuit is isolated from the DGND of the digital circuit by a 0Ω resistor. The capacitor of the power supply pin and the filter capacitor of the audio signal should also be connected to AUDIO_GND.

6.10.UART interface

ECK20-6Y2XA core board supports up to 8 asynchronous serial ports and a baud rate of up to 5.0Mbps. The core board uses UART 1 as the debug serial port by default.

6.11.SPI interface

The ECK20-6Y2XA series core board supports up to 4 SPI controllers and supports master/slave mode. SPI signals include SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. When designing, you must first confirm the relationship between the master and slave devices, and then confirm the direction of the MOSI and MISO signals. 1 SPI can only connect to 1 device.

6.12.I2C interface

The ECK20-6Y2XA series core board supports 4-way I2C controllers and 2 clock frequency modes. The rate in standard mode is 100Kbit/s and the rate in fast mode is 400Kbit/s.

Several devices can be mounted on the same I2C bus. The following points should be noted when designing the schematic:

a) Check whether the device addresses on the same bus conflict;

b) Ensure that each I2C bus has a pair of pull-up resistors. The recommended resistance is 2.2K~10K, but do not add multiple resistors.

c) The core board provides I2C bus pull-up resistors, which require users to pull up when using the baseboard;

d) Check whether the I2C interface level of the device is 3.3V. If not, a level conversion circuit needs to be added;

e) Check whether the I2C interface power rails are consistent. When I2C interfaces in different time domains are interconnected, the bus switch circuit needs to be considered;

f) Do not use too many devices on the same bus, otherwise the load capacitance limit of 400pF required by the I2C specification may be exceeded, affecting the signal waveform.

6.13.CAN interface

The ECK20-6Y2XA series core board supports 2-way CAN controllers and CAN protocol specification version 2.0 B. It only needs an external CAN transceiver to perform CAN communication.

6.14.ADC interface

The ECK20-6Y2XA series core board can provide up to 10 ADC input channels and has a 12-bit ADC converter. The ADC reference voltage VREF uses the internal reference of the p

rocessor.

6.15.GPIO interface

The ECK20-6Y2XA series core board can provide up to 105 GPIO interfaces, but most of them have multiplexing functions. Users can flexibly configure GPIO according to their own needs.

6.16.Hardware design checklist

- ❖Power rail: Check whether there is an inconsistency in the power rails of the I/O interface application, such as a 1.8V signal connected to a 3.3V signal. If there is a need to connect signals with different power rails, a level conversion circuit should be used.
- ❖Power-on sequence: Check whether the signals connecting the baseboard and the core board are powered on first, or whether the power-on time of the two board signals is very different.
- ❖Pull-up and pull-down resistors: The output state of the multiplexed I/O interface is uncertain before the power-on software configuration. If the signal needs to maintain a certain level when powered on, pull-up and pull-down resistors should be designed on the baseboard. Some functional signals also need to be designed with pull-up or pull-down resistors on the baseboard, such as I2C signals. When designing pull-up resistors, attention should be paid to the design of the pull-up power rail.
- ❖ESD protection: The corresponding ESD protection design should be considered for the external interface signal. The selection of ESD solution should take into account the requirements of signal rate, communication protocol and application environment.
- ❖High-speed signals should be of equal length: High-speed signals should consider the equal length design of PCB, including USB, Ethernet, SDIO, display, etc.
- ❖Impedance control: High-speed signals should consider PCB impedance control. The key to impedance control is to maintain impedance continuity. The baseboard should be designed with reference to the impedance of the core board signal.

7. Software Resources

The ECK20-6Y2XA series core board is equipped with an operating system based on the Linux 5.10.9 kernel. The development board comes with a cross-compilation tool chain required for embedded Linux system development, U-boot source code, source code for the Linux kernel and various driver modules, as well as various development and debugging tools suitable for Windows desktop environment and Linux desktop environment.

operating system:

Ubuntu 20.04 system

System source code:

u-boot 2020.04

Kernel 5.10.9

Yocto gatesgarth

Development environment and tools:

Burning tool: uuu

Configuration Tools: Config Tools for i.MX V15

7.1.System resources

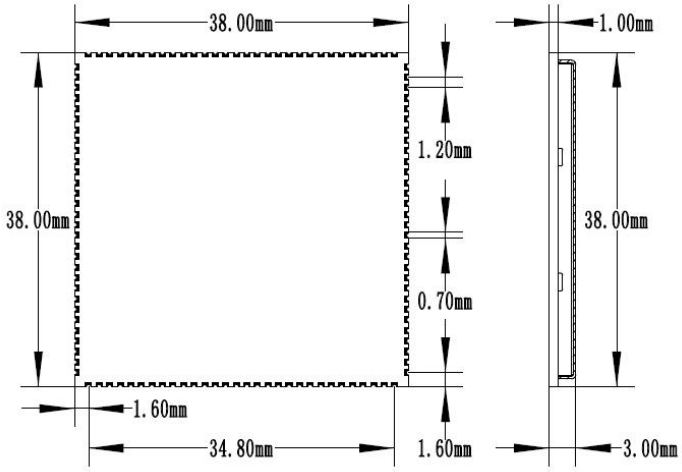
System Software Resource Table

category	name	describe	Source code
BOOT	u-boot 2020.04	Bootloader	/source/u-boot_2020.04.tar.xz
Kernel	Kernel 5.10.9	Linux Kernel	/source/kernel_5.10.9.tar.xz
Device Driver	MMC	eMMC/TF card driver	drivers/mmc/host/sdhci-esdhc-imx.c
	NAND	MTD Driver	drivers/mtd/nand/raw/gpmi-nand/gpmi-nand.c
	SPI	SPI Driver	drivers/spi/spi-imx.c
	I2C	I2C Driver	drivers/i2c/busses/i2c-imx.c
	USB Host	USB Drivers	drivers/usb/host/ohci-platform.c
	Ethernet	Network Drivers	drivers/net/ethernet/freescale/fec_main.c
	UART	Serial port driver	drivers/tty/serial/imx.c
	Can bus	Can bus driver	drivers/net/can/flexcan.c
	GPIO keys	Key Driver	drivers/input/keyboard/gpio_keys.c
	RTC	RTC Driver	drivers/rtc/rtc-snvs.c
	GPIO LED	Led Driver	drivers/leds/leds-gpio.c
	LCD	LCDIF Driver	drivers/video/fbdev/mxsfb.c
	Resistive touch	ADC touch driver	drivers/input/touchscreen/imx6ul_tsc.c
operating	Rootfs	Ubuntu 20.04 system	/images/rootfs.tar.bz2

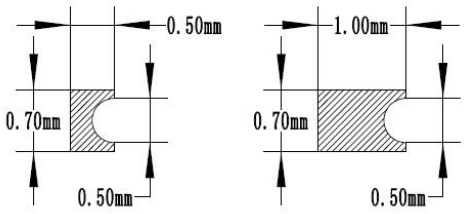
system			
Development Tools	Yocto gatesgarth	Operating system build	/source/yocto-gatesgarth.tar
	Gcc	Cross-compilation tools	/tools/gcc-linaro-7.5.0-2019.12-x86_64_arm-linux-gnueabihf.tar.xz
	uuu	Burning tool	/tools/uuu
	Config Tools for i.MX	Resource Configuration Tools	/tools/Config_Tools_for_i.MX_v15_x64.exe
	balenaEtcher	SD boot card creation tool	/tools/balenaEtcher-Portable-1.18.11.exe

8. Structural Dimensions

The ECK20-6Y2XA series core board adopts 120 PIN, 1.2mm pitch stamp hole interface, which can be STM soldered or hand soldered. There are no components on the bottom of the core board, no exposed wiring, and the bottom board design is simple. The core board structure size is shown in the figure below.



Stamp hole core board structure size drawing



Stamp hole size chart

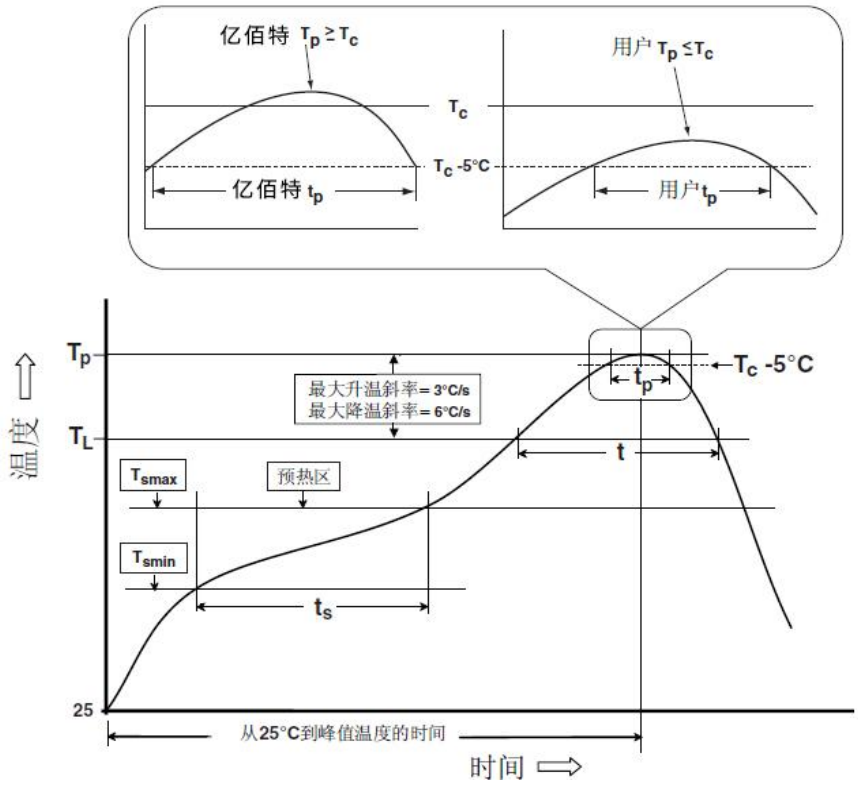
9. Welding Instructions

9.1.Reflow temperature

Reflow Temperature Table

Reflow profile characteristics		Leaded process assembly	Lead-free assembly
Preheating/keeping	Minimum temperature (Tsmin)	100℃	150℃
	Maximum temperature (Tsmax)	150℃	200℃
	Time (Tsmin~Tsmin)	60-120 seconds	60-120 seconds
Heating slope (TL~Tp)		3℃/sec, max.	3℃/sec, max.
Liquidus temperature (TL)		183℃	217℃
Keep time above TL		60~ 90 seconds	60~ 90 seconds
Package peak temperature Tp		Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.	Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.
The time (Tp) within 5°C of the specified classification temperature (Tc) is shown in the figure below.		20 seconds	30 seconds
Cooling slope (Tp~TL)		6℃/sec, max.	6℃/sec, max.
Time from room temperature to peak temperature		6 minutes, longest	8 minutes, longest
※The peak temperature (Tp) tolerance of the temperature curve is defined as the upper limit of the user			

9.2.Reflow oven profile



Reflow Oven Profile

10. Reference Documentation

IMX6ULLIEC.pdf

IMX6ULLRM.pdf

Chip Errata for the i.MX 6ULL.pdf

11. Revision Notes

Revision Notes Table

Version	Modifications	Modification time	prepared by	Proofreading	Approval
V1.0	First Draft	24-08-09	WFX	WYQ	WFX

About us

Technical support: service@cdebyte.com

Documents and RF Setting download link: www.cdebyte.com

Thank you for using Ebyte products! Please contact us with any questions or suggestions: info@cdebyte.com

---

Web: www.cdebyte.com

Address: B5 Mould Park, 199# Xiqu Ave, High-tech District, Sichuan, China

Chengdu Ebyte Electronic Technology Co.,Ltd.