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8051-Based MCU

MG82F6D17/
MG82F6D003
Brief Datasheet

Version: 1.00

2021/02 version 1.00

Features

- 1-T 80C51 Central Processing Unit
- **MG82F6D17/6D003** with **16K** Bytes flash ROM
  - ISP memory zone could be optioned as **0.5KB/1.0KB~7.5KB**
  - Flexible IAP size by software configured
  - Code protection for flash memory access
  - Flash write/erase cycle: 20,000
  - Flash data retention: 100 years at 25°C
- **Default MG82F6D17/6D003 Flash space mapping**
  - AP Flash default mapping (13.5KB, 0000h~35FFh)
  - IAP Flash default mapping (1.0KB, 3600h~39FFh)
  - ISP Flash default mapping (1.5KB, 3A00h~3FFFh), ISP Boot code
- Data RAM: **1K** Bytes
  - On-chip 256 bytes scratch-pad RAM
  - **768** bytes expanded RAM (XRAM) for **MG82F6D17/6D003**
  - Support page select on XRAM access in **MG82F6D17/6D003**
- Dual data pointer
- Provide one channel DMA engine
  - P2P, M2P, P2M
  - Memory target: XRAM
  - Peripheral target: UART0, UART1, SPI, TWI0/I2C0, ADC12 & CRC16
  - Timer 5 and Timer 6 are used for DMA, but it also can be traded as independent timer when DMA not in use
- Interrupt controller
  - **16** sources, four-level-priority interrupt capability
  - **Three** external interrupt inputs, nINT0, nINT1 and nINT2 with glitch filter
  - All external interrupts support High/Low level or Rising/Falling edge trigger
- Total **9/11** timers in **MG82F6D17/6D003**
  - RTC Timer and WDT Timer
  - Timer 0, Timer 1, Timer 2 and Timer 3
  - PCA0, Program Counter Array 0
  - S0 BRG and S1 BRG
  - If Timer 2/3 in split mode, total **11** timers
- **Four** 16-bit timer/counters, Timer 0, Timer 1, Timer 2 and Timer 3
  - X12 mode and timer clock output function
  - Synchronous Run-Enable on all timer (same function on Stop and Reload)
  - New 5 operating modes in Timer 2/3 with 8 clock sources and 8 capture sources
  - Timer 2/3 can be split to two 8-bit timers
  - Clock Count Output (CCO) on T2CKO and T3CKO
  - All timers support PWM mode
- **One** Programmable 16-bit counter/timer Arrays (PCA0) with **8** Compare/PWM modules
  - PCA0 has 6 CCP (Capture/Compare/PWM) modules and 2 CP (Compare/PWM) modules
  - Reloadable 16-bit base counter to support variable length PWM
  - Up to **144 MHz** clock source from on-chip CKM
  - Capture mode, 16-bit software timer mode and High speed output mode
  - Buffered capture mode to monitor narrow pulse input
  - Variable 8/10/12/16-bit PWM mode, the PCA can be configured to:
    - Up to **8** channels un-buffered 10/12/16-bit PWM, or

    - ∗ Up to **8** channels buffered 2~8-bit PWM, or
    - ∗ Up to **4** channels buffered 9~16-bit PWM
  - — PCA0 PWM module 0~5 with dead-time control, break control and central-aligned option
- 8 Inputs Keypad Interrupt
- 12-Bit Single-ended ADC
  - — Programmable throughput up to **800K** sps
  - — 8 channel external inputs and one channel internal input (IVR/1.4V)
  - — Support window detect function on ADC result
  - — Support channel scan mode
- Enhanced UART (S0)
  - — Framing Error Detection
  - — Automatic Address Recognition
  - — Max. UART baud rate up to 3.6864MHz/ 6MHz
  - — Support SPI Master in Mode 4, up to 12MHz on SPICLK
  - — Built-in baud rate generator (S0BRG) to support TX or RX on different baud rate
  - — Support LIN bus protocol with auto baud rate detection in mode 5
  - — S0BRG in timer mode cascaded with Timer 0/1 to be a 16/24-bit timer/counter
- Secondary UART (S1)
  - — Dedicated Baud Rate Generator (S1BRG) shares to S0 or set as an 8-bit timer
  - — Max. UART baud rate up to 1.8432/3.0MHz
  - — Support SPI Master in Mode 4, up to 12MHz on SPICLK
  - — S1BRG in timer mode cascaded with Timer 0/1 to be a 16/24-bit timer/counter
- One Master/Slave SPI serial interface
  - — Max. 24MHz SPICLK on SPI master
  - — Max 12MHz on SPI slave
  - — 8 bits data transfer
  - — Up to 3 SPI masters including S0/S1 in mode 4
  - — Support daisy-chain function in SPI slave mode
- Two Master/Slave two wire serial interfaces: TWI0/ I2C0 and STWI (SI2C)
  - — One Master/Slave hardware engine: TWI0/ I2C0
  - — Max. 1MHz on TWI0/ I2C0 master mode and Max. 400KHz on TWI0 slave mode
  - — One software TWI/ I2C, STWI/ SI2C, Start/Stop serial interface detection (SID)
- Programmable Watchdog Timer (WDT), clock sourced from ILRCO or SYSCLK/12
  - — One time enabled by CPU or power-on
  - — Interrupt CPU or Reset CPU on WDT overflow
  - — Support WDT function in power down mode (watch mode) for auto-wakeup function
- Real-Time-Clock (RTC) module, clock sourced from ILRCO, WDTPS, WDTOF, SYSCLK or SYSCLK/12
  - — Programmable interrupt period from mini-second wakeup to minute wakeup
  - — 21-bit length system timer
- Beeper function
- General purpose logic (GPL/CRC)
  - — Bit order reversed function
  - — 16-bit CRC engine (CCITT-16 polynomial)
  - — Support automatic CRC of flash content
  - — Programmable initial seed function of CRC
- On-Chip-Debug interface (OCD)
  - — **MG82F6D17AS8** SOP8 not support OCD
- Maximum **17** GPIOs in 20-pin package
  - — P3 can be configured to quasi-bidirectional, push-pull output, open-drain output and input only
  - — P0, P1, P2, P4 and P6 can be configured to open-drain output or push-pull output

  - P4.7 shared with RST
  - Programmable GPIO driving strength and driving speed
  - On chip pull-up enabled on each pin
- Clock Sources
  - Internal 12MHz/11.059MHz oscillator (IHRCO): factory calibrated to ±1%, typical
  - Internal Low power 32KHz RC Oscillator (ILRCO)
  - External clock input (ECKI) on P6.0, up to 25MHz
  - Internal RC Oscillator output on P6.0
  - On-chip Clock Multiplier (CKM) to provide high speed clock source (144 MHz)
- Two Brown-Out Detectors
  - BOD0: detect **1.7V**
  - BOD1: selected detection level on 4.2V/3.7V/2.4V/2.0V
  - Interrupt CPU or reset CPU
  - Wake up CPU in Power-Down mode (BOD1)
- Multiple power control modes: idle mode, power-down mode, slow mode, sub-clock mode, RTC mode, watch mode and monitor mode.
  - All interrupts can wake up IDLE mode
  - **12(13)** sources with **16** pins to wake up Power-Down mode
  - Slow mode and sub-clock mode support low speed MCU operation
  - RTC mode supports RTC to resume CPU in power down
  - Watch mode supports WDT to resume CPU in power down
  - Monitor mode supports BOD1 to resume CPU in power down
- Operating voltage range: 1.8V – 5.5V
  - Minimum **1.8V** requirement in flash write operation (ISP/IAP/ICP)
- Operation frequency range: **32** (max)
  - External clock input mode, 0 – 12MHz @ 2.0V – 5.5V, 0 – 25MHz @ 2.4V – 5.5V
  - CPU up to 12MHz @ **1.8V** – 5.5V, and up to 25MHz @ **2.2V** – 5.5V
  - **CPU up to 36MHz @ 2.7V -5.5V with on-chip CKM**
- 16-Bytes Unique ID code
- Operating Temperature:
  - Industrial (-40°C to +105°C)*
- Package Types:
  - SOP8 (150 mil): MG82F6D17AS8 (16K)
  - SSOP20 (150 mil): MG82F6D17AL20 (16K)
  - TSSOP20 (173 mil): MG82F6D17AT20 (16K), MG82F6D003AT20 (16K)
  - QFN20 (3 x 3 x 0.55 mm): MG82F6D17AZ20 (16K)

*: Tested by sampling.

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1. General Description

The **MG82F6D17/6D003** is a single-chip microcontroller based on a high performance 1-T architecture 80C51 CPU that executes instructions in 1~7 clock cycles (about 6~7 times the rate of a standard 8051 device), and has an 8051 compatible instruction set. Therefore at the same performance as the standard 8051, the **MG82F6D17/6D003** can operate at a much lower speed and thereby greatly reduce the power consumption.

The **MG82F6D17/6D003** has **16K** bytes of embedded Flash memory for code and data. The Flash memory can be programmed either in serial writer mode (via ICP, In-Circuit Programming) or in In-System Programming mode. And, it also provides the In-Application Programming (IAP) capability. ICP and ISP allow the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-volatile data in the Flash memory while the application program is running. There needs no external high voltage for programming due to its built-in charge-pumping circuitry.

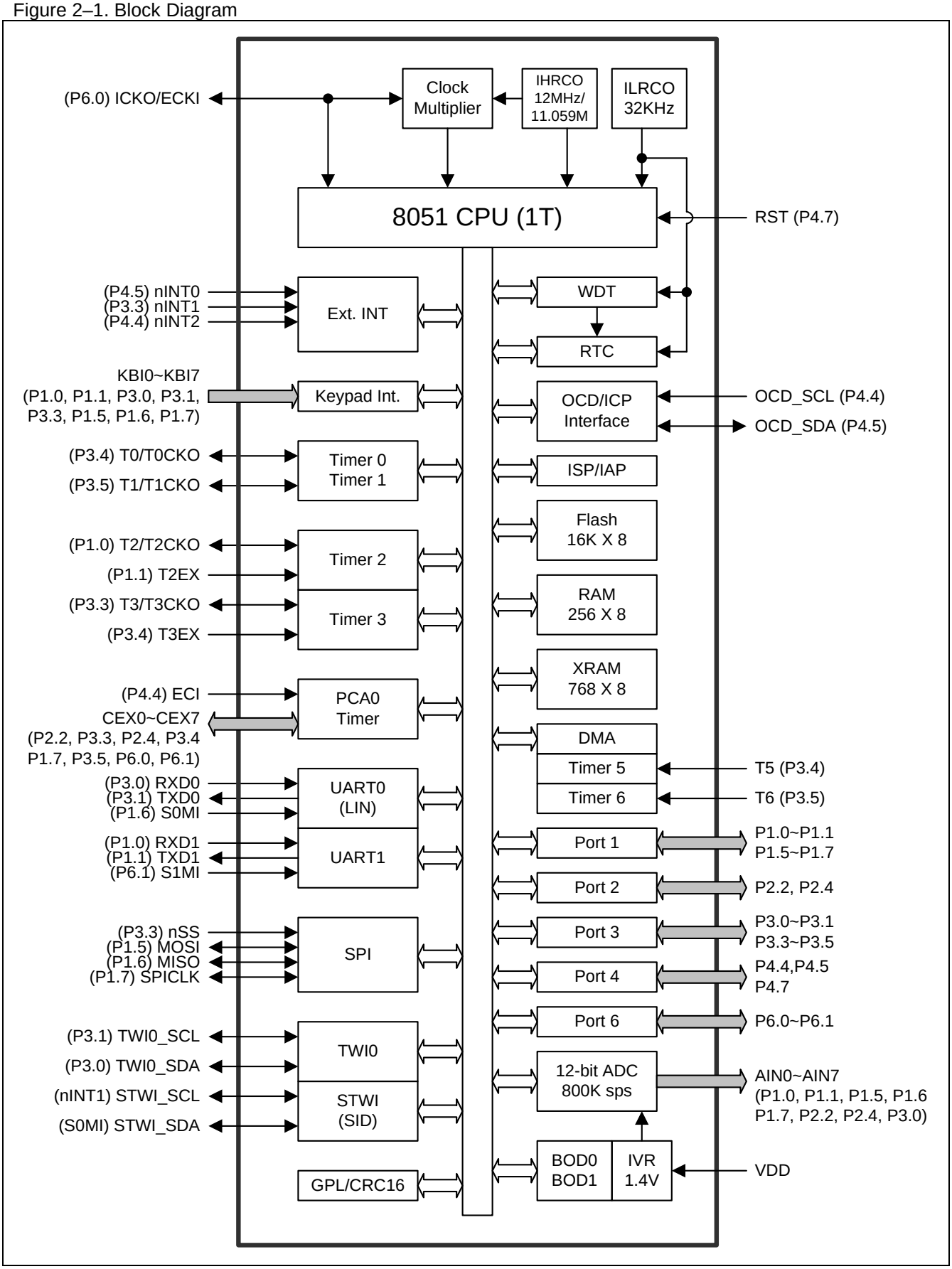
The **MG82F6D17/6D003** retains all features of the standard 80C52 with 256 bytes of scratch-pad RAM, two external interrupts, a multi-source 4-level interrupt controller, a serial port (UART0) and three timer/counters. In addition, the **MG82F6D17/6D003** has17 I/O port pins, one XRAM of 768 bytes, one extra external interrupts with High/low trigger option, 800KHz 12-bit ADC, one 16-bit timer, one 8-channel PCA with dead-time controlled PWM, one 8-bit SPI, two TWI/ I2C (TWI0/ I2C0 and STWI/ SI2C), secondary serial port (UART1), keypad interrupt, Watchdog Timer, Real-Time-Clock module, two Brown-out Detectors, an ECKI external clock input (P6.0), an internal high precision oscillator (IHRCO), an on-chip clock multiplier (CKM) to generate high speed clock source, an internal low speed RC oscillator (ILRCO) and an enhanced serial function in UART0 that facilitates multiprocessor communication, LIN bus mode and a speed improvement mechanism (X2/X4 mode). Support 3 different DMA transfer types, M2P (XRAM to Peripheral), P2M (Peripheral to XRAM) and P2P (Peripheral to Peripheral) to enhance transfer performance and reduce CPU loading.

The **MG82F6D17/6D003** has multiple operating modes to reduce the power consumption: idle mode, power down mode, slow mode, sub-clock mode, RTC mode, watch mode and monitor mode. In the Idle mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the Power-Down mode the RAM and SFRs' value are saved and all other functions are inoperative; most importantly, in the Power-down mode the device can be waked up by many interrupt or reset sources. In slow mode, the user can further reduce the power consumption by using the 8-bit system clock pre-scaler to slow down the operating speed. Or select sub-clock mode which clock source is derived from internal low speed oscillator (ILRCO) for CPU to perform an ultra-low speed operation. The RTC module supports Real-Time-Clock function in all operating modes. In watch mode, it keeps WDT running in power-down or idle mode and resumes CPU as an auto-wakeup timer when WDT overflows. Monitor mode provides the Brown-Out detection in power down mode and resumes CPU when chip VDD reaches the specific detection level.

Additionally, the **MG82F6D17/6D003** is equipped with the Megawin proprietary On-Chip Debug (OCD) interface for In-Circuit Emulator (ICE). The OCD interface provides on-chip and in-system non-intrusive debugging without any target resource occupied. Several operations necessary for an ICE are supported such as Reset, Run, Stop, Step, Run to Cursor and Breakpoint Setting. The user has no need to prepare any development board during firmware developing or the socket adapter used in the traditional ICE probe head. All the thing the user needs to do is to prepare a connector for the dedicated OCD interface. This powerful feature makes the developing very easy for any user.

2. Block Diagram

Figure 2–1. Block Diagram



3. Special Function Register

3.1. SFR Map (Page 0~F)

		0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8	0	*P6*	CH	CCAP0H	CCAP1H	CCAP2H	CCAP3H	CCAP4H	CCAP5H
	1			CCAP6H	CCAP7H				
F0	0	*B*	PAOE	PCAPWM0	PCAPWM1	PCAPWM2	PCAPWM3	PCAPWM4	PCAPWM5
	1			PCAPWM6	PCAPWM7				
E8	0	*P4*	CL	CCAP0L	CCAP1L	CCAP2L	CCAP3L	CCAP4L	CCAP5L
	1			CCAP6L	CCAP7L				
E0	0	*ACC*	WDTCR	IFD	IFADRH	IFADRL	IFMT	SCMD	ISPCR
	1								
D8	0	*CCON*	CMOD	CCAPM0	CCAPM1	CCAPM2	CCAPM3	CCAPM4	CCAPM5
	1			CCAPM6	CCAPM7				
D0	0	*PSW*	SIADR	SIDAT	SISTA	SICON	KBPATN	KBCON	KBMASK
	1								
C8	0	*T2CON*	T2MOD	RCAP2L	RCAP2H	TL2	TH2	CLRL	CHRL
	1	*T3CON*	T3MOD	RCAP3L	RCAP3H	TL3	TH3		
	3	*T5CON*	--	TLR5	THR5	TL5	TH5		
	4	*T6CON*	--	TLR6	THR6	TL6	TH6		
C0	0	*XICON*	XICFG	--	ADCFG0	ADCON0	ADCDL	ADCDH	CKCON0
	1		XICFG1		ADCFG1				
	2		--		ADCFG2				
	3				ADCFG3				
	4				ADCFG4				
	5				ADCFG5				
	B				ADCFG11				
	C				ADCFG12				
	D				ADCFG13				
	E				ADCFG14				
B8	0	*IP0L*	SADEN/ S0CR1	--	--	PWMCR	CRC0DA	RTCCR	--
	1					PDTCRA			
B0	0	*P3*	P3M0	P3M1	P4M0	--	--	RTCTM	IP0H
	1				--	--	P6M0		
	2				--	PDRVC0	--		
	3				--	PDRVC1	--		
A8	0	*IE*	SADDR	--	--	SFRPI	EIE1	EIP1L	EIP1H
	1								
A0	0	*P2*	AUXR0	AUXR1	AUXR2	AUXR3	EIE2	EIP2L	EIP2H
	1					AUXR4			
	2					AUXR5			
	3					AUXR6			
	4					AUXR7			
	5					AUXR8			
	6					AUXR9			
	7					AUXR10			
	8					AUXR11			
98	0	*S0CON*	S0BUF	S0BRT	S0BRC	S0CFG	S0CFG1		
	1	*S1CON*	S1BUF	S1BRT	S1BRC	S1CFG			
90	0	*P1*	P1M0	P1M1	--	DMACR0	P2M0	BOREV	PCON1
	1			P2M1	T2MOD1	DMACR0	TREN0		
	2			P4M1	T3MOD1	DMACR0	TRLC0		
	3			P6M1	--	DMACR0	TSPC0		
	4			--	--	DMACR0	--		
	5			--	--	DMACR0	--		
	6			--	--	DMACR0	--		
	7			P3FDC	--	DMACR0	--		
	8			P1FDC	--	DMACG0	--		
	9			P2FDC	--	DMADS0	--		
	A			P4FDC	--	--	--		
88	0	*TCON*	TMOD	TL0	TL1	TH0	TH1	SFIE	XRPS
	1								
80	0	--	SP	DPL	DPH	SPSTAT	SPCON	SPDAT	PCON0
	1								
		0/8	**1/9**	**2/A**	**3/B**	**4/C**	**5/D**	**6/E**	**7/F**

***: User needs to set SFRPI as SFRPI=0x00 ~ 0x0F for SFR page access.**
（MCU will not keep SFRPI value in interrupt. User need to keep SFRPI value in software flow.）

SFRPI: SFR Page Index Register

SFR Page = 0~F

SFR Address = 0xAC RESET = xxxx-0000

7	6	5	4	3	2	1	0
--	--	--	--	IDX3	IDX2	IDX1	IDX0
W	**W**	**W**	**W**	**R/W**	**R/W**	**R/W**	**R/W**

Bit 7~4: Reserved. Software must write “0” on these bits when SFRPI is written.

Bit 3~0: SFR Page Index.

PIDX[3:0]	Selected Page
0000	Page 0
0001	Page 1
0010	Page 2
0011	Page 3
……	……
……	……
……	……
1111	Page F

3.2. SFR Bit Assignment (Page 0~F)

Table 3–1. SFR Bit Assignment (Page 0~F)

SYMBOL	DESCRIPTION	ADDR	BIT ADDRESS AND SYMBOL								RESET VALUE
			Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
SP	Stack Pointer	81H	.7	.6	.5	.4	.3	.2	.1	.0	00000111
DPL	Data Pointer Low	82H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
DPH	Data Pointer High	83H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
SPSTAT	SPI Status Register	84H	SPIF	WCOL	THRF	SPIBSY	MODF	--	--	SPR2	00000xx0
SPCON	SPI Control Register	85H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	00000100
SPDAT	SPI Data Register	86H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
PCON0	Power Control 0	87H	SMOD1	SMOD0	GF	POF0	GF1	GF0	PD	IDL	00010000
TCON	*Timer Control*	*88H*	*TF1*	*TR1*	*TF0*	*TR0*	*IE1*	*IT1*	*IE0*	*IT0*	*00000000*
TMOD	Timer Mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00000000
TL0	Timer Low 0	8AH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TL1	Timer Low 1	8BH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TH0	Timer High 0	8CH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TH1	Timer High 1	8DH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
SFIE	System Flag INT En.	8EH	SIDFIE	--	--	RTCFIE	--	BOF1IE	BOF0IE	WDTFIE	0000x000
XRPS	XRAM Page Select	8FH	--	--	--	--	--	--	.1	.0	xxxxx000
P1	*Port 1*	*90H*	*P1.7*	*P1.6*	*P1.5*	--	--	--	*P1.1*	*P1.0*	*11111111*
P1M0	P1 Mode Register 0	91H	P1M0.7	P1M0.6	P1M0.5	--	--	--	P1M0.1	P1M0.0	00000000
P1M1	P1 Mode Register 1	92H	P1M1.7	P1M1.6	P1M1.5	--	--	--	P1M1.1	P1M1.0	11111111
P2M1	P2 Mode Register 1	92H	--	--	--	P2M1.4	--	P2M1.2	--	--	11111111
P4M1	P4 Mode Register 1	92H	P4M1.7	--	P4M1.5	P4M1.4	--	--	--	--	11111111
P6M1	P6 Mode Register 1	92H	--	--	--	--	--	--	P6M1.1	P6M1.0	11111111
P3FDC	P3 Fast Drv. Ctrl.	92H	--	--	.5	.4	.3	--	.1	.0	00000000
P1FDC	P1 Fast Drv. Ctrl.	92H	.7	.6	.5	--	--	--	.1	.0	00000000
P2FDC	P2 Fast Drv. Ctrl.	92H	--	--	--	.4	--	.2	--	--	00000000
P4FDC	P4 Fast Drv. Ctrl.	92H	.7	--	.5	.4	--	--	--	--	00000000
T2MOD1	Timer2 mode 1 Reg.	93H	TL2CS	TF2IG	TL2IS	T2CKS	T2MS1	CP2S2	CP2S1	CP2S0	00000000
T3MOD1	Timer3 mode 1 Reg.	93H	TL3CS	TF3IG	--	T3CKS	T3MS1	CP3S2	CP3S1	CP3S0	00x00000
DMACR0	DMA Control Reg. 0	94H	--	--	--	--	DMAE0	DMAS0	DIE0	DCF0	xxx00000
DMACG0	DMA Configured Reg. 0	94H	PDMAH	PDMAL	CRCW0	0	EXTS10	EXTS00	FAEN0	LOOP0	00000000
DMADS0	DMA Data path Selection 0	94H	DSS30	DSS20	DSS10	DSS00	DDS30	DDS20	DDS10	DDS00	00000000
P2M0	P2 Mode Register 0	95H	--	--	--	P2M0.4	--	P2M0.2	--	--	00000000
TREN0	Timer Run Enable Register 0	95H	--	TR3LE	TR2LE	--	TR3E	TR2E	TR1E	TR0E	x00x0000
TRLC0	Timer Reload Control Register 0	95H	--	TL3RLC	TL2RLC	--	T3RLC	T2RLC	T1RLC	T0RLC	x00x0000
TSPC0	Timer Stop Control Register 0	95H	--	TL3SC	TL2SC	--	T3SC	T2SC	T1SC	T0SC	x00x0000
BOREV	Bit Order Reversed	96H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
PCON1	Power Control 1	97H	SWRF	EXRF	--	RTCF	--	BOF1	BOF0	WDTF	0000x000
S0CON	*Serial 0 Control*	*98H*	*SM00 /FE*	*SM10*	*SM20*	*REN0*	*TB80*	*RB80*	*TI0*	*RI0*	*00000000*
S1CON	*Serial 1 Control*	*98H*	*SM01*	*SM11*	*SM21*	*REN1*	*TB81*	*RB81*	*TI1*	*RI1*	*00000000*
S0BUF	Serial 0 Buffer	99H	.7	.6	.5	.4	.3	.2	.1	.0	xxxxxxxx
S1BUF	Serial 1 Buffer	99H	.7	.6	.5	.4	.3	.2	.1	.0	xxxxxxxx
S0BRT	S0 Baud-Rate Timer	9AH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
S1BRT	S1 Baud-Rate Timer	9AH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
S0BRC	S0 Baud-Rate Counter	9BH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
S1BRC	S1 Baud-Rate Counter	9BH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
S0CFG	S0 Configuration	9CH	URTS	SMOD2	URM0X3	SM30	S0DOR	BTI	UTIE	SMOD3	00001000
S1CFG	S1 Configuration	9CH	SM31	S1M0X3	S1DOR	S1TR	S1MOD1	S1TX12	S1CKOE	S1TME	00100000
S0CFG1	S0 Configuration 1 (LINCFG)	9DH	SBF0	TXER0	S0SB16	ATBR0	TXRX0	SYNC0	--	--	000000xx
P2	*Port 2*	*A0H*	--	--	--	*P2.4*	--	*P2.2*	--	--	*11111111*
AUXR0	Auxiliary Register 0	A1H	P60OC1	P60OC0	P60FD	PBKF	--	--	INT1H	INT0H	00000000
AUXR1	Auxiliary Register 1	A2H	--	--	CRCDS1	CRCDS0	--	--	--	DPS	00000000
AUXR2	Auxiliary Register 2	A3H	STAF	STOF	--	--	T1X12	T0X12	T1CKOE	T0CKOE	00000000
AUXR3	Auxiliary Register 3	A4H	T0PS1	T0PS0	BPOC1	BPOC0	S0PS0	TWIPS1	TWIPS0	T0XL	00000000
AUXR4	Auxiliary Register 4	A4H	T2PS1	T2PS0	T1PS1	T1PS0	--	--	--	--	00000000
AUXR5	Auxiliary Register 5	A4H	C0IC4S0	C0IC2S0	C0PPS1	C0PPS0	--	C0PS0	ECIPS0	C0COPS	00000000
AUXR6	Auxiliary Register 6	A4H	KBI4PS1	KBI4PS0	KBI6PS0	KBI2PS0	T3FCS	T2FCS	SnMIPS	S0COPS	00000000
AUXR7	Auxiliary Register 7	A4H	POE5	POE4	C0CKOE	SPI0M0	--	--	--	--	11000000
AUXR8	Auxiliary Register 8	A4H	POE7	POE6	C0PPS2	--	KBI0PS0	S1COPS	--	--	11000000
AUXR9	Auxiliary Register 9	A4H	--	--	T1G1	T0G1	C0FDC1	C0FDC0	S1PS1	S1PS0	00000000
AUXR10	Aux. Register 10	A4H	--	--	--	SPIPS0	S0PS1	--	TWICF	PAA	00000000
AUXR11	Aux. Register 11	A4H	P30AM	--	--	--	--	--	C0M0	C0OFS	00000000
EIE2	Extended INT Enable 2	A5H	--	--	--	--	--	--	--	ET3	xxxxxxx0

SYMBOL	DESCRIPTION	ADDR	BIT ADDRESS AND SYMBOL								RESET
			Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	VALUE
EIP2L	Ext. INT Priority 2 Low	A6H	--	--	--	--	--	--	--	PT3L	xxxxxxx0
EIP2H	Ext. INT Priority 2 High	A7H	--	--	--	--	--	--	--	PT3H	xxxxxxx0
IE	*Interrupt Enable*	*A8H*	*EA*	*EDMA*	*ET2*	*ES0*	*ET1*	*EX1*	*ET0*	*EX0*	*00000000*
SADDR	Slave Address	A9H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
SFRPI	SFR Page Index	ACH	--	--	--	--	IDX3	IDX2	IDX1	IDX0	xxx00000
EIE1	Extended INT Enable 1	ADH	--	ETWI0	EKB	ES1	ESF	EPCA	EADC	ESPI	00000000
EIP1L	Ext. INT Priority 1 Low	AEH	--	PTWI0L	PKBL	PS1L	PSFL	PPCAL	PADCL	PSPIL	00000000
EIP1H	Ext. INT Priority 1 High	AFH	--	PTWI0H	PKBH	PS1H	PSFH	PPCAH	PADCH	PSPIH	00000000
P3	*Port 3*	*B0H*	--	--	*P3.5*	*P3.4*	*P3.3*	--	*P3.1*	*P3.0*	*11111111*
P3M0	P3 Mode Register 0	B1H	--	--	P3M0.5	P3M0.4	P3M0.3	--	P3M0.1	P3M0.0	00000000
P3M1	P3 Mode Register 1	B2H	--	--	P3M1.5	P3M1.4	P3M1.3	--	P3M1.1	P3M1.0	00000000
P4M0	P4 Mode Register 0	B3H	P4M0.7	--	P4M0.5	P4M0.4	--	--	--	--	10110000
PDRVC0	Port Driving Control 0	B4H	P3DC1	P3DC0	P2DC1	P2DC0	P1DC1	P1DC0	--	--	00000000
PDRVC1	Port Driving Control 1	B4H	--	--	--	--	--	--	P4DC1	--	xxx0xx00
P6M0	P6 Mode Register 0	B5H	--	--	--	--	--	--	P6M0.1	P6M0.0	00000000
RTCTM	RTC Timer Register	B6H	RTCCS1	RTCCS0	RTCCT5	RTCCT4	RTCCT3	RTCCT2	RTCCT1	RTCCT0	01111111
IP0H	Interrupt Priority 0 High	B7H	--	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	00000000
IP0L	*Interrupt Priority Low*	*B8H*	--	*PX2L*	*PT2L*	*PSL*	*PT1L*	*PX1L*	*PT0L*	*PX0L*	*00000000*
SADEN	Slave Address Mask	B9H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
S0CR1	S0 Control 1	B9H	S0TR	S0TX12	S0TCK	S0RCK	S0CKOE	ARTE	--	--	00000000
PWMCR	PWM Control Reg.	BCH	PCAE	EXDT	PBKM	PBKE1.1	PBKE1.0	PBKE0.2	PBKE0.1	PBKE0.0	00000000
PDTCRA	PWM Dead-Time Control Reg. -A	BCH	DTPS1	DTPS0	DT.5	DT.4	DT.3	DT.2	DT.1	DT.0	00000000
CRC0DA	CRC0 Data Port	BDH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
RTCCR	RTC Control Reg.	BEH	RTCE	RTCO	RTCRL5	RTCRL4	RTCRL3	RTCRL2	RTCRL1	RTCRL0	00111111
XICON	*External INT Control*	*C0H*	--	--	--	--	*INT2H*	*EX2*	*IE2*	*IT2*	*xxxx0000*
XICFG	Ext. INT. Configured	C1H	INT1IS1	INT1IS0	INT0IS1	INT0IS0	--	X2FLT	X1FLT	X0FLT	00000000
XICFG1	Ext. INT. Configured 1	C1H	INT1IS2	INT0IS2	INT2IS1	INT2IS0	--	X2FLT1	X1FLT1	X0FLT1	00000000
ADCFG0	ADC Configuration 0	C3H	ADCKS2	ADCKS1	ADCKS0	ADRJ	ACHS	SMPF	ADTM1	ADTM0	00000000
ADCFG1	ADC Configuration 1	C3H	IGADCI	EADCWI	SMPFIE	SIGN	AOS.3	AOS.2	AOS.1	AOS.0	00000000
ADCFG2	ADC Configuration 2	C3H	SHT.7	SHT.6	SHT.5	SHT.4	SHT.3	SHT.2	SHT.1	SHT.0	00000000
ADCFG3	ADC Configuration 3	C3H	ADPS1	ADPS0	--	--	ARES1	ARES0	ADES0	--	010000xx
ADCFG4	ADC Configuration 4	C3H	--	ADWM0	ADTM3	ADTM2	--	--	DBSD	--	0000xx00
ADCFG5	ADC Configuration 5	C3H	ASCE.7	ASCE.6	ASCE.5	ASCE.4	ASCE.3	ASCE.2	ASCE.1	ASCE.0	00000000
ADCFG11	ADC Configuration 11	C3H	WHB.3	WHB.2	WHB.1	WHB.0	1	1	1	1	11111111
ADCFG12	ADC Configuration 12	C3H	WHB.11	WHB.10	WHB.9	WHB.8	WHB.7	WHB.6	WHB.5	WHB.4	11111111
ADCFG13	ADC Configuration 13	C3H	WLB.3	WLB.2	WLB.1	WLB.0	0	0	0	0	00000000
ADCFG14	ADC Configuration 14	C3H	WLB.11	WLB.10	WLB.9	WLB.8	WLB.7	WLB.6	WLB.5	WLB.4	00000000
ADCON0	ADC Control 0	C4H	ADCEN	ADCWI	--	ADCI	ADCS	CHS2	CHS1	CHS0	0x000000
ADCDL	ADC Data Low	C5H	ADCV.3	ADCV.2	ADCV.1	ADCV.0	--	--	--	--	0000xxxx
ADCDH	ADC Data High	C6H	ADCV.11	ADCV.10	ADCV.9	ADCV.8	ADCV.7	ADCV.6	ADCV.5	ADCV.4	00000000
CKCON0	Clock Control 0	C7H	AFS	ENCKM	CKMIS1	CKMIS0	CCKS	SCKS2	SCKS1	SCKS0	00010000
T2CON	*Timer 2 Control Reg.*	*C8H*	*TF2*	*EXF2*	*RCLK/ TF2L*	*TCLK/ TL2IE*	*EXEN2*	*TR2*	*C/T2*	*CP/RL2*	*00000000*
T3CON	*Timer 3 Control Reg.*	*C8H*	*TF3*	*EXF3*	*TF3L*	*TL3IE*	*EXEN3*	*TR3*	*C/T3*	*CP/RL3*	*00000000*
T5CON	*Timer 5 Control Reg.*	*C8H*	*TF5*	--	*T5CKS1*	*T5CKS0*	*T5IE*	*TR5*	*T5GAT1*	*T5GAT0*	*00000000*
T6CON	*Timer 6 Control Reg.*	*C8H*	*TF6*	--	*T6CKS1*	*T6CKS0*	*T6IE*	*TR6*	*T6GAT1*	*T6GAT0*	*00000000*
T2MOD	Timer 2 mode Reg.	C9H	T2SPL	TL2X12	T2EXH	T2X12	TR2L	TR2LC	T2OE	T2MS0	00000000
T3MOD	Timer 3 mode Reg.	C9H	T3SPL	TL3X12	T3EXH	T3X12	TR3L	TR3LC	T3OE	T3MS0	00000000
RCAP2L	Timer2 Capture Low	CAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
RCAP3L	Timer3 Capture Low	CAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TLR5	TL5 reload Reg.	CAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TLR6	TL6 reload Reg.	CAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
RCAP2H	Timer2 Capture High	CBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
RCAP3H	Timer3 Capture High	CBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
THR5	TH5 reload Reg.	CBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
THR6	TH6 reload Reg.	CBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TL2	Timer Low 2	CCH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TL3	Timer Low 3	CCH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TL5	Timer Low 5	CCH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TL6	Timer Low 6	CCH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TH2	Timer High 2	CDH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TH3	Timer High 3	CDH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TH5	Timer High 5	CDH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
TH6	Timer High 6	CDH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CLRL	CL Reload register	CEH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CHRL	CH Reload register	CFH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
PSW	*Program Status Word*	*D0H*	*CY*	*AC*	*F0*	*RS1*	*RS0*	*OV*	*F1*	*P*	*00000000*
SIADR	TWI0 Address Reg.	D1H	.7	.6	.5	.4	.3	.2	.1	GC	00000000
SIDAT	TWI0 Data Reg.	D2H	.7	.6	.5	.4	.3	.2	.1	.0	00000000

SYMBOL	DESCRIPTION	ADDR	BIT ADDRESS AND SYMBOL								RESET
			Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	VALUE
SISTA	TWI0 Status Reg.	D3H	.7	.6	.5	.4	.3	.2	.1	.0	11111000
SICON	TWI0 Control Reg.	D4H	CR2	ENSI	STA	STO	SI	AA	CR1	CR0	00000000
KBPATN	Keypad Pattern	D5H	.7	.6	.5	.4	.3	.2	.1	.0	11111111
KBCON	Keypad Control	D6H	KBCS1	KBCS0	KBES	--	--	--	PATN_SEL	KBIF	00000001
KBMASK	Keypad Int. Mask	D7H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCON	*PCA Control Reg.*	*D8H*	*CF*	*CR*	*CCF5*	*CCF4*	*CCF3*	*CCF2*	*CCF1*	*CCF0*	*00000000*
CMOD	PCA Mode Reg.	D9H	CIDL	BME4	BME2	BME0	CPS2	CPS1	CPS0	ECF	00000000
CCAPM0	PCA Module0 Mode	DAH	DTE0	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	00000000
CCAPM6	PCA Module6 Mode	DAH	BME6	ECOM6	--	CAPN6	MAT6	TOG6	PWM6	ECCF6	00xx0000
CCAPM1	PCA Module1 Mode	DBH	--	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x0000000
CCAPM7	PCA Module7 Mode	DBH	--	ECOM7	--	CAPN7	MAT7	TOG7	PWM7	ECCF7	x0xx0000
CCAPM2	PCA Module2 Mode	DCH	DTE2	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	00000000
CCAPM3	PCA Module3 Mode	DDH	--	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x0000000
CCAPM4	PCA Module4 Mode	DEH	DTE4	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	00000000
CCAPM5	PCA Module5 Mode	DFH	--	ECOM5	CAPP5	CAPN5	MAT5	TOG5	PWM5	ECCF5	x0000000
ACC	*Accumulator*	*E0H*	*ACC.7*	*ACC.6*	*ACC.5*	*ACC.4*	*ACC.3*	*ACC.2*	*ACC.1*	*ACC.0*	*00000000*
WDTCR	WDT Control register	E1H	WREN	NSW	ENW	CLRW	WIDL	PS2	PS1	PS0	00000000
IFD	ISP Flash data	E2H	.7	.6	.5	.4	.3	.2	.1	.0	11111111
IFADRH	ISP Flash Addr. High	E3H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
IFADRL	ISP Flash Addr. Low	E4H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
IFMT	ISP Mode Table	E5H	MS.7	--	--	--	MS.3	MS.2	MS.1	MS.0	00000000
SCMD	ISP Serial Command	E6H	.7	.6	.5	.4	.3	.2	.1	.0	xxxxxxxx
ISPCR	ISP Control Register	E7H	ISPEN	SWBS	SRST	CFAIL	--	--	--	--	00000xxx
P4	*Port 4*	*E8H*	*P4.7*	--	*P4.5*	*P4.4*	--	--	--	--	*11111111*
CL	PCA base timer Low	E9H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP0L	PCA module0 capture Low	EAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP6L	PCA module6 capture Low	EAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP1L	PCA module1 capture Low	EBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP7L	PCA module7 capture Low	EBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP2L	PCA module2 capture Low	ECH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP3L	PCA module3 capture Low	EDH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP4L	PCA module4 capture Low	EEH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP5L	PCA module5 capture Low	EFH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
B	*B Register*	*F0H*	*B.7*	*B.6*	*B.5*	*B.4*	*B.3*	*B.2*	*B.1*	*B.0*	*00000000*
PAOE	PWM Additional Output Enable	F1H	POE3	POE2B	POE2A	POE2	POE1	POE0B	POE0A	POE0	10011001
PCAPWM0	PCA PWM0 Mode	F2H	P0RS1	P0RS0	--	--	--	P0INV	ECAP0H	ECAP0L	00xxx000
PCAPWM6	PCA PWM6 Mode	F2H	P6RS1	P6RS0	--	--	CCF6	P6INV	ECAP6H	ECAP6L	00xx0000
PCAPWM1	PCA PWM1 Mode	F3H	P1RS1	P1RS0	--	--	--	P1INV	ECAP1H	ECAP1L	00xxx000
PCAPWM7	PCA PWM7 Mode	F3H	P7RS1	P7RS0	--	--	CCF7	P7INV	ECAP7H	ECAP7L	00xx0000
PCAPWM2	PCA PWM2 Mode	F4H	P2RS1	P2RS0	--	--	--	P2INV	ECAP2H	ECAP2L	00xxx000
PCAPWM3	PCA PWM3 Mode	F5H	P3RS1	P3RS0	--	--	--	P3INV	ECAP3H	ECAP3L	00xxx000
PCAPWM4	PCA PWM4 Mode	F6H	P4RS1	P4RS0	--	--	--	P4INV	ECAP4H	ECAP4L	00xxx000
PCAPWM5	PCA PWM5 Mode	F7H	P5RS1	P5RS0	--	--	--	P5INV	ECAP5H	ECAP5L	00xxx000
P6	*Port 6*	*F8H*	--	--	--	--	--	--	*P6.1*	*P6.0*	*xxx11111*
CH	PCA base timer High	F9H	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP0H	PCA Module0 capture High	FAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP6H	PCA Module6 capture High	FAH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP1H	PCA Module1 capture High	FBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP7H	PCA Module7 capture High	FBH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP2H	PCA Module2 capture High	FCH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP3H	PCA Module3 capture High	FDH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP4H	PCA Module4 capture High	FEH	.7	.6	.5	.4	.3	.2	.1	.0	00000000
CCAP5H	PCA Module5 capture High	FFH	.7	.6	.5	.4	.3	.2	.1	.0	00000000

3.3. Auxiliary SFR Map (Page P)

MG82F6D17/6D003 has an auxiliary SFR page which is indexed by page P and the SFRs' write is a different way from standard 8051 SFR page. The registers in auxiliary SFR map are addressed by IFMT and SCMD like ISP/IAP access flow. Page P has 256 bytes space that can target to **11 physical bytes** and **6 logical bytes.** IAPLB, CKCON2, CKCON3, CKCON4, CKCON5, PCON2, PCON3, SPCON0, DCON0, RTCTM and RTCCR. The 6 logical bytes include PCON0, PCON1, CKCON0, WDTCR, P4 and P6. Access on the 6 logical bytes gets the coherence content with the same SFR in Page 0~F.

Table 3–2. Auxiliary SFR Map (Page P)

		0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8		P6	--	--	--	--	--	--	--
F0		--	--	--	--	--	--	--	--
E8		P4	--	--	--	--	--	--	--
E0		--	WDTCR	--	--	--	--	--	--
D8		--	--	--	--	--	--	--	--
D0		--	--	--	--	--	--	--	--
C8		--	--	--	--	--	--	--	--
C0		--	--	--	--	--	--	--	CKCON0
B8		--	--	--	--	--	--	--	--
B0		--	--	--	--	--	--	--	--
A8		--	--	--	--	--	--	--	--
A0		--	--	--	--	--	--	--	--
98		--	--	--	--	--	--	--	--
90		--	--	--	--	--	--	--	PCON1
88		--	--	--	--	--	--	--	--
80		--	--	--	--	--	--	--	PCON0
78		--	--	--	--	--	--	--	--
70		--	--	--	--	--	--	--	--
68		--	--	--	--	--	--	--	--
60		--	--	--	--	--	--	--	--
58		--	--	--	--	--	--	--	--
50		--	--	--	--	RTCCR	RTCTM	--	--
48		SPCON0	--	--	--	DCON0	--	--	--
40		CKCON2	CKCON3	CKCON4	CKCON5	PCON2	PCON3	--	--
38		--	--	--	--	--	--	--	--
30		--	--	--	--	--	--	--	--
28		--	--	--	--	--	--	--	--
20		--	--	--	--	--	--	--	--
18		--	--	--	--	--	--	--	--
10		--	--	--	--	--	--	--	--
08		--	--	--	--	--	--	--	--
00		--	--	--	IAPLB	--	--	--	--
		0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F

3.4. Auxiliary SFR Bit Assignment (Page P)

Table 3–3. Auxiliary SFR Bit Assignment (Page P)

SYMBOL	DESCRIPTION	ADDR	BIT ADDRESS AND SYMBOL								RESET VALUE
			Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Physical Bytes											
IAPLB	IAP Low Boundary	03H	IAPLB6	IAPLB5	IAPLB4	IAPLB3	IAPLB2	IAPLB1	IAPLB0	0	
CKCON2	Clock Control 2	40H	--	--	--	IHRCOE	MCKS1	MCKS0	OSCS1	OSCS0	0001-0000
CKCON3	Clock Control 3	41H	WDTCS1	WDTCS0	FWKP	WDTFS	MCKD1	MCKD0	--	--	00000000
CKCON4	Clock Control 4	42H	RCSS2	RCSS1	RCSS0	RPSC2	RPSC1	RPSC0	RTCCS3	RTCCS2	00000000
CKCON5	Clock Control 5	43H	--	--	--	--	--	--	--	CKMS0	00000000
PCON2	Power Control 2	44H	AWBOD1	0	BO1S1	BO1S0	BO1RE	EBOD1	BO0RE	1	0000x1x1
PCON3	Power Control 3	45H	IVREN	0	0	0	0	0	0	0	00000000
SPCON0	SFR Page Control 0	48H	--	P6CTL	P4CTL	WRCTL	--	CKCTL0	PWCTL1	PWCTL0	00000000
DCON0	Device Control 0	4CH	HSE	IAPO	HSE1	--	--	IORCTL	RSTIO	OCDE	100xx011
RTCCR	RTC Control Reg.	54H	RTCE	RTCO	RTCRL5	RTCRL4	RTCRL3	RTCRL2	RTCRL1	RTCRL0	00111111
RTCTM	RTC Timer Register	55H	RTCCS1	RTCCS0	RTCCT5	RTCCT4	RTCCT3	RTCCT2	RTCCT1	RTCCT0	01111111
Logical Bytes											
PCON0	Power Control 0	87H	SMOD1	SMOD0	GF	POF0	GF1	GF0	PD	IDL	00010000
PCON1	Power Control 1	97H	SWRF	EXRF	--	RTCF	--	BOF1	BOF0	WDTF	0000x000
CKCON0	Clock Control 0	C7H	AFS	ENCKM	CKMIS1	CKMIS0	CCKS	SCKS2	SCKS1	SCKS0	00010000
WDTCR	Watch-dog-timer Control register	E1H	WREN	NSW	ENW	CLRW	WIDL	PS2	PS1	PS0	00000000
P4	Port 4	E8H	P4.7	--	P4.5	P4.4	--	--	--	--	1x11xx11
P6	Port 6	F8H	--	--	--	--	--	--	P6.1	P6.0	xxxxxx11

Sample Code of Page-P SFR write：

```
IFADRH = 0x00;
ISPCR = ISPEN;                  //enable IAP/ISP
IFMT = MS2;                     // Page-P write，IFMT =0x04
IFADRL = SPCON0;                //Set Page-P SFR address
IFD |= CKCTL0;                  // set CKCTL0
SCMD = 0x46;                    //
SCMD = 0xB9;                    //
IFMT = Flash_Standby;           // IAP/ISP standby，IFMT =0x00
ISPCR &= ~ISPEN;
```

4. Pin Configurations

4.1. MG82F6D17 Package Instruction

Figure 4–1. SSOP20 Top View

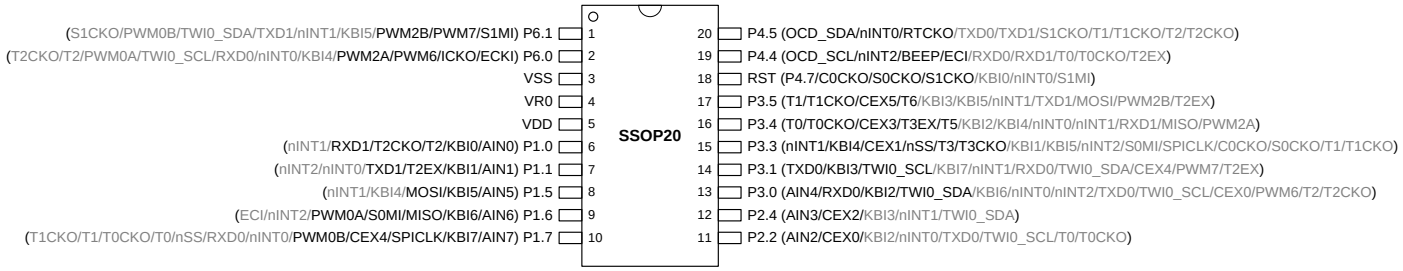


Figure 4–2. TSSOP20 Top View

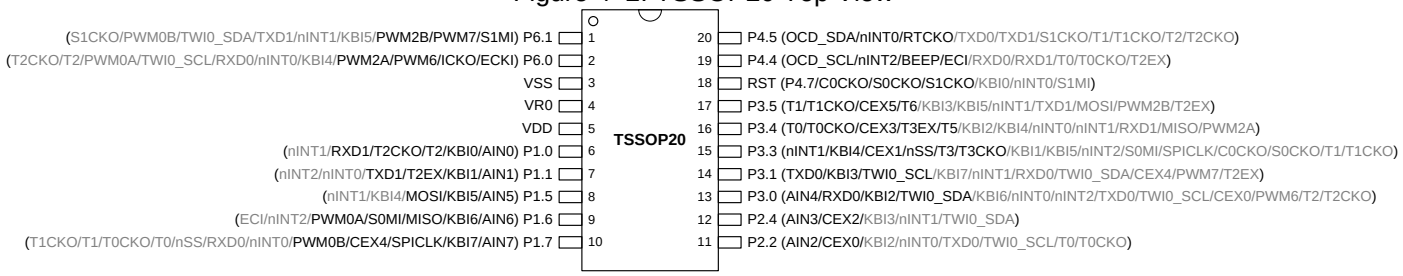


Figure 4–3. QFN20 Top View

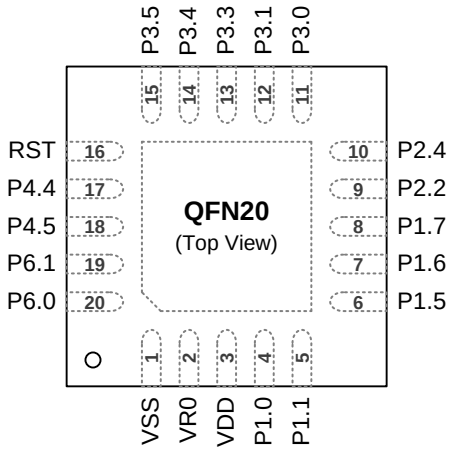
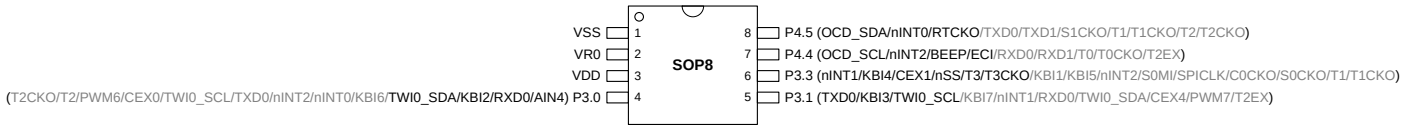


Figure 4–4. SOP8 Top View

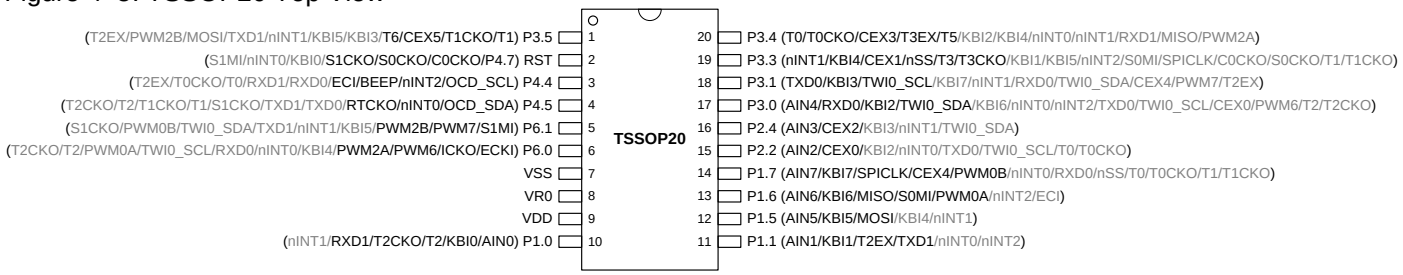


Note: For MG82F6D17AS8 SOP8

1. *Does not support OCD ICE or ICP*
2. *P4.4 and P4.5 is used for OCD function as default mode, please disable OCD_ICE in the initial step of the firmware.*

4.2. MG82F6D003 Package Instruction

Figure 4–5. TSSOP20 Top View



4.3. Pin Description

Table 4–1. Pin Description of MG82F6D17

MNEMONIC	PIN NUMBER				I/O TYPE	DESCRIPTION
	20-Pin SSOP	20-Pin TSSOP	20-Pin QFN	8-Pin SOP		
P1.0 (AIN0) (KBI0) (T2) (T2CKO) (RXD1)	6	6	4		I/O	* Port 1.0. * AIN0: ADC channel-0 analog input. * KBI0: keypad input 0. * T2: Timer/Counter 2 external clock input. * T2CKO: Timer 2 programmable clock output. * RXD1: UART1 serial input port.
P1.1 (AIN1) (KBI1) (T2EX) (TXD1)	7	7	5		I/O	* Port 1.1. * AIN1: ADC channel-1 analog input. * KBI1: keypad input 1. * T2EX: Timer/Counter 2 external control input. * TXD1: UART1 serial output port.
P1.5 (AIN5) (KBI5) (MOSI)	8	8	6		I/O	* Port 1.5. * AIN5: ADC channel-5 analog input. * KBI5: keypad input 5. * MOSI: SPI master out & slave in.
P1.6 (AIN6) (KBI6) (MISO) (S0MI) (PWM0A)	9	9	7		I/O	* Port 1.6. * AIN6: ADC channel-6 analog input. * KBI6: keypad input 6. * MISO: SPI master in & slave out. * S0MI: Serial Port 0 SPI Master mode data Input. * PWM0A: PCA PWM0 output sub-channel A.
P1.7 (AIN7) (KBI7) (SPICLK) (CEX4) (PWM0B)	10	10	8		I/O	* Port 1.7. * AIN7: ADC channel-7 analog input. * KBI7: keypad input 7. * SPICLK: SPI clock, output for master and input for slave. * CEX4: PCA0 module-4 external I/O. * PWM0B: PCA0 PWM0 output sub-channel B.
P2.2 (AIN2) (CEX0)	11	11	9		I/O	* Port 2.2. * AIN2: ADC channel-2 analog input. * CEX0: PCA0 module-0 external I/O.
P2.4 (AIN3) (CEX2)	12	12	10		I/O	* Port 2.4. * AIN3: ADC channel-3 analog input. * CEX2: PCA0 module-2 external I/O.
P3.0 (AIN4) (RXD0) (KBI2) (TWI0_SDA)	13	13	11	4	I/O	* Port 3.0. * AIN4: ADC channel-4 analog input. * RXD0 : UART0 serial input port. * KBI2: keypad input 2. * TWI0_SDA: serial data of TWI0/ I2C0.
P3.1 (TXD0) (KBI3) (TWI0_SCL)	14	14	12	5	I/O	* Port 3.1. * TXD0 : UART0 serial output port. * KBI3: keypad input 3. * TWI0_SCL: serial clock of TWI0/ I2C0.
P3.3 (nINT1) (KBI4) (CEX1) (nSS) (T3) (T3CKO)	15	15	13	6	I/O	* Port 3.3. * nINT1: external interrupt 1 input. * KBI4: keypad input 4. * CEX1: PCA0 module-1 external I/O. * nSS: SPI Slave select. * T3: Timer/Counter 3 external clock input. * T3CKO: Timer 3 programmable clock output.
P3.4 (T0) (T0CKO) (CEX3) (T3EX) (T5)	16	16	14		I/O	* Port 3.4. * T0: Timer/Counter 0 external input. * T0CKO: Timer 0 programmable clock output. * CEX3: PCA0 module-3 external I/O. * T3EX: Timer/Counter 3 external control input. * T5: Timer/Counter 5 external clock input.

MNEMONIC	PIN NUMBER				I/O TYPE	DESCRIPTION
	20-Pin SSOP	20-Pin TSSOP	20-Pin QFN	8-Pin SOP		
P3.5 (T1) (T1CKO) (CEX5) (T6)	17	17	15		I/O	* Port 3.5. * T1: Timer/Counter 1 external input. * T1CKO: Timer 1 programmable clock output. * CEX5: PCA0 module-5 external I/O. * T6: Timer/Counter 6 external clock input.
P4.4 (OCD_SCL) (nINT2) (BEEP) (ECI)	19	19	17	7	I/O	* Port 4.4. * OCD_SCL: OCD interface, serial clock. (Need to disable by firmware of MG82F6D17AS8 SOP8) * nINT2: external interrupt 2 input. * BEEP: Beeper output. * ECI: PCA external clock input.
P4.5 (OCD_SDA) (nINT0) (RTCKO)	20	20	18	8	I/O	* Port 4.5. * OCD_SDA: OCD interface, serial data. (Need to disable by firmware of MG82F6D17AS8 SOP8) * nINT0: external interrupt 0 input. * RTCKO: RTC programmable clock output.
P6.0 (ECKI) (ICKO) (PWM6) (PWM2A)	2	2	20		I/O I O	* Port 6.0. * ECKI: In external clock input mode, this is clock input pin. * ICKO: Internal Clock (MCK) Output. * PWM6: PCA0 module-6 PWM6 output. * PWM2A: PCA0 PWM2 output sub-channel A.
P6.1 (S1MI) (PWM7) (PWM2B)	1	1	19		I/O	* Port 6.1. * S1MI: Serial Port 1 SPI Master mode data Input. * PWM7: PCA0 module-7 PWM7 output. * PWM2B: PCA0 PWM2 output sub-channel B.
RST (P4.7) (C0CKO) (S0CKO) (S1CKO)	18	18	16		I I/O	* RST: External RESET input, high active. * Port 4.7. * C0CKO: Programmable clock output of PCA base counter. * S0CKO: S0BRT programmable clock output. * S1CKO: S1BRG programmable clock output.
VR0	4	4	2	2	I/O	* VR0. Voltage Reference 0. Connect 0.1uF and 4.7uF to VSS.
VDD	5	5	3	3	P	Power supply input.
VSS	3	3	1	1	G	Ground, 0 V reference.

Table 4–2. Pin Description of MG82F6D003

MNEMONIC	PIN NUMBER 20-Pin TSSOP	I/O TYPE	DESCRIPTION
P1.0 (AIN0) (KBI0) (T2) (T2CKO) (RXD1)	10	I/O	* Port 1.0. * AIN0: ADC channel-0 analog input. * KBI0: keypad input 0. * T2: Timer/Counter 2 external clock input. * T2CKO: Timer 2 programmable clock output. * RXD1: UART1 serial input port.
P1.1 (AIN1) (KBI1) (T2EX) (TXD1)	11	I/O	* Port 1.1. * AIN1: ADC channel-1 analog input. * KBI1: keypad input 1. * T2EX: Timer/Counter 2 external control input. * TXD1: UART1 serial output port.
P1.5 (AIN5) (KBI5) (MOSI)	12	I/O	* Port 1.5. * AIN5: ADC channel-5 analog input. * KBI5: keypad input 5. * MOSI: SPI master out & slave in.
P1.6 (AIN6) (KBI6) (MISO) (S0MI) (PWM0A)	13	I/O	* Port 1.6. * AIN6: ADC channel-6 analog input. * KBI6: keypad input 6. * MISO: SPI master in & slave out. * S0MI: Serial Port 0 SPI Master mode data Input. * PWM0A: PCA PWM0 output sub-channel A.
P1.7 (AIN7) (KBI7) (SPICLK) (CEX4) (PWM0B)	14	I/O	* Port 1.7. * AIN7: ADC channel-7 analog input. * KBI7: keypad input 7. * SPICLK: SPI clock, output for master and input for slave. * CEX4: PCA0 module-4 external I/O. * PWM0B: PCA0 PWM0 output sub-channel B.
P2.2 (AIN2) (CEX0)	15	I/O	* Port 2.2. * AIN2: ADC channel-2 analog input. * CEX0: PCA0 module-0 external I/O.
P2.4 (AIN3) (CEX2)	16	I/O	* Port 2.4. * AIN3: ADC channel-3 analog input. * CEX2: PCA0 module-2 external I/O.
P3.0 (AIN4) (RXD0) (KBI2) (TWI0_SDA)	17	I/O	* Port 3.0. * AIN4: ADC channel-4 analog input. * RXD0 : UART0 serial input port. * KBI2: keypad input 2. * TWI0_SDA: serial data of TWI0/ I2C0.
P3.1 (TXD0) (KBI3) (TWI0_SCL)	18	I/O	* Port 3.1. * TXD0 : UART0 serial output port. * KBI3: keypad input 3. * TWI0_SCL: serial clock of TWI0/ I2C0.
P3.3 (nINT1) (KBI4) (CEX1) (nSS) (T3) (T3CKO)	19	I/O	* Port 3.3. * nINT1: external interrupt 1 input. * KBI4: keypad input 4. * CEX1: PCA0 module-1 external I/O. * nSS: SPI Slave select. * T3: Timer/Counter 3 external clock input. * T3CKO: Timer 3 programmable clock output.
P3.4 (T0) (T0CKO) (CEX3) (T3EX) (T5)	20	I/O	* Port 3.4. * T0: Timer/Counter 0 external input. * T0CKO: Timer 0 programmable clock output. * CEX3: PCA0 module-3 external I/O. * T3EX: Timer/Counter 3 external control input. * T5: Timer/Counter 5 external clock input.
P3.5 (T1) (T1CKO) (CEX5) (T6)	1	I/O	* Port 3.5. * T1: Timer/Counter 1 external input. * T1CKO: Timer 1 programmable clock output. * CEX5: PCA0 module-5 external I/O. * T6: Timer/Counter 6 external clock input.

MNEMONIC	PIN NUMBER 20-Pin TSSOP	I/O TYPE	DESCRIPTION
P4.4 **(OCD_SCL)** **(nINT2)** **(BEEP)** **(ECI)**	3	I/O	* Port 4.4. * OCD_SCL: OCD interface, serial clock. (Need to disable by firmware of MG82F6D17/6D003AS8 SOP8) * nINT2: external interrupt 2 input. * BEEP: Beeper output. * ECI: PCA external clock input.
P4.5 **(OCD_SDA)** **(nINT0)** **(RTCKO)**	4	I/O	* Port 4.5. * OCD_SDA: OCD interface, serial data. (Need to disable by firmware of MG82F6D17/6D003AS8 SOP8) * nINT0: external interrupt 0 input. * RTCKO: RTC programmable clock output.
P6.0 **(ECKI)** **(ICKO)** **(PWM6)** **(PWM2A)**	6	I/O I O	* Port 6.0. * ECKI: In external clock input mode, this is clock input pin. * ICKO: Internal Clock (MCK) Output. * PWM6: PCA0 module-6 PWM6 output. * PWM2A: PCA0 PWM2 output sub-channel A.
P6.1 **(S1MI)** **(PWM7)** **(PWM2B)**	5	I/O	* Port 6.1. * S1MI: Serial Port 1 SPI Master mode data Input. * PWM7: PCA0 module-7 PWM7 output. * PWM2B: PCA0 PWM2 output sub-channel B.
RST **(P4.7)** **(C0CKO)** **(S0CKO)** **(S1CKO)**	2	I I/O	* RST: External RESET input, high active. * Port 4.7. * C0CKO: Programmable clock output of PCA base counter. * S0CKO: S0BRT programmable clock output. * S1CKO: S1BRG programmable clock output.
VR0	8	I/O	* VR0. Voltage Reference 0. Connect 0.1uF and 4.7uF to VSS.
VDD	9	P	Power supply input.
VSS	7	G	Ground, 0 V reference.

4.4. Alternate Function Redirection

Many I/O pins, in addition to their normal I/O function, also serve the alternate function for internal peripherals. For the digital peripherals, all GPIOs serve the alternate function in the default state. However, the user may set the corresponding control bits in AXUR0~AUXR3 to serve their alternate function on the relocated ports.

AUXR0: Auxiliary Register 0

SFR Page = 0~F

SFR Address = 0xA1 RESET = 0000-0000

7	6	5	4	3	2	1	0
P60OC1	P60OC0	P60FD	PBKF	--	--	INT1H	INT0H
R/W	**R/W**	**R/W**	**R/W**	**W**	**W**	**R/W**	**R/W**

Bit 7~6: P6.0 function configured control bit 1 and 0. The two bits only act when internal RC oscillator (IHRCO or ILRCO) is selected for system clock source. In external clock input mode, P6.0 is the dedicated clock input pin. In internal oscillator condition, P6.0 provides the following selections for GPIO or clock source generator. When P60OC[1:0] index to non-P6.0 GPIO function, P6.0 will drive the on-chip RC oscillator output to provide the clock source for other devices.

P60OC[1:0]	P60 function	I/O mode
00	P60	By P6M0.0
01	MCK	By P6M0.0
10	MCK/2	By P6M0.0
11	MCK/4	By P6M0.0

For clock-out on P6.0 function, it is recommended to set P6M0.0 to “1” which selects P6.0 as push-push output mode.

Bit 5: P60FD, P6.0 Fast Driving.
0: P6.0 output with default driving.
1: P6.0 output with fast driving enabled. If P6.0 is configured to clock output, enable this bit when P6.0 output frequency is more than 12MHz at 5V application or more than 6MHz at 3V application.

AUXR3: Auxiliary Register 3

SFR Page = **0 only**

SFR Address = 0xA4 RESET = 0000-0000

7	6	5	4	3	2	1	0
T0PS1	T0PS0	BPOC1	BPOC0	S0PS0	TWIPS1	TWIPS0	T0XL
R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**

Bit 7~6: T0PS1~0, Timer 0 Port pin Selection [1:0].

T0PS1~0	T0/T0CKO
00	P3.4
01	P4.4
10	P2.2
11	P1.7

Bit 3: S0PS0, Serial Port 0 pin Selection 0. (Add new S0PS1 at AUXR10.3)

S0PS1~0	RXD0	TXD0
00	P3.0	P3.1
01	P4.4	P4.5
10	P3.1	P3.0
11	P1.7	P2.2

Bit 2~1: TWIPS1~0, TWI0/I2C0 Port pin Selection [1:0].

TWIPS1~0	TWI0_SCL	TWI0_SDA
00	P3.1	P3.0
01	P6.0	P6.1
10	P3.0	P3.1
11	P2.2	P2.4

AUXR4: Auxiliary Register 4

SFR Page = **1 only**
SFR Address = 0xA4 RESET = 0000-0000

7	6	5	4	3	2	1	0
T2PS1	T2PS0	T1PS1	T1PS0	--	--	--	--
R/W	**R/W**	**R/W**	**R/W**	**W**	**W**	**W**	**W**

Bit 7~6: T2PS1~0, Timer 2 Port pin Selection [1:0].

T2PS1~0	T2/T2CKO	T2EX
00	P1.0	P1.1
01	P3.0	P3.1
10	P6.0	P3.5
11	P4.5	P4.4

Bit 5~4: T1PS1~0, Timer 1 Port pin Selection [1:0].

T1PS1~0	T1/T1CKO
00	P3.5
01	P4.5
10	P1.7
11	P3.3

AUXR5: Auxiliary Register 5
SFR Page = **2 only**
SFR Address = 0xA4 RESET = 0000-0000

7	6	5	4	3	2	1	0
C0IC4S0	C0IC2S0	C0PPS1	C0PPS0	--	C0PS0	ECIPS0	C0COPS
R/W	**R/W**	**R/W**	**R/W**	**W**	**R/W**	**R/W**	**R/W**

Bit 7: C0IC4S0, PCA0 Input Channel 4 input port pin Selection.

C0IC4S0	CEX4 input
0	CEX4 Port Pin
1	T2EXI

Bit 6: C0IC2S0, PCA0 Input Channel 2 input port pin Selection.

C1IC2S0	CEX2 input
0	CEX2 Port Pin
1	T3EXI

Bit 5: C0PPS1, {PWM2A, PWM2B} Port pin Selection 1.

C0PPS1	PWM2A	PWM2B
0	P6.0	P6.1
1	P3.4	P3.5

Bit 4: C0PPS0, {PWM0A, PWM0B} Port pin Selection 0.

C0PPS0	PWM0A	PWM0B
0	P1.6	P1.7
1	P6.0	P6.1

Bit 3: Reserved.

Bit 2: C0PS0, PCA0 Port pin Selection 0.

C0PS0	CEX0	*CEX2*	CEX4
0	P2.2	*P2.4*	P1.7
1	P3.0	*P2.4*	P3.1

Bit 1: ECIPS0, PCA0 ECI Port pin Selection0.

ECIPS0	ECI
0	P4.4
1	P1.6

Bit 0: C0COPS, PCA0 Clock Output (C0CKO) port pin Selection.

C0COPS	C0CKO
0	P4.7
1	P3.3

AUXR6: Auxiliary Register 6

SFR Page = **3 only**

SFR Address = 0xA4 RESET = 0000-0000

7	6	5	4	3	2	1	0
KBI4PS1	KBI4PS0	KBI6PS0	KBI2PS0	T3FCS	T2FCS	SnMIPS	S0COPS
R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**

Bit 7~6: KBI4PS1~0, KBI4~5 Port pin Selection [1:0].

KBI4PS1~0	KBI4	KBI5
00	P3.3	P1.5
01	P3.4	P3.5
10	P6.0	P6.1
11	P1.5	P3.3

Bit 5: KBI6PS0, KBI6~7 Port pin Selection 0.

KBI6PS0	KBI6	KBI7
0	P1.6	P1.7
1	P3.0	P3.1

Bit 4: KBI2PS0, KBI2~3 Port pin Selection 0.

KBI2PS0	KBI2	KBI3
0	P3.0	P3.1
1	P2.2	P2.4

Bit 3: T3FCS, Reserved for chip test.

Bit 2: T2FCS, Reserved for chip test.

Bit 1: SnMIPS, S0MI & S1MI Port pin Selection.

SnMIPS	S0MI	S1MI
0	P1.6	P6.1
1	P3.3	P4.7

Bit 0: S0COPS, S0BRG Clock Output (S0CKO) port pin Selection.

S0COPS	S0CKO
0	P4.7
1	P3.3

AUXR7: Auxiliary Register 7

SFR Page = **4 only**

SFR Address = 0xA4 RESET = 1100-0000

7	6	5	4	3	2	1	0
POE5	POE4	C0CKOE	SPI0M0	--	--	--	--
R/W	**R/W**	**R/W**	**R/W**	**W**	**W**	**W**	**W**

Bit 7: POE5, PCA0 PWM5 main channel (PWM5O) output control.
0: Disable PWM5O output on port pin.
1: Enable PWM5O output on port pin. **Default is enabled.**

Bit 6: POE4, PCA0 PWM4 main channel (PWM4O) output control.
0: Disable PWM4O output on port pin.
1: Enable PWM4O output on port pin. **Default is enabled.**
Bit 5: C0CKOE, PCA0 clock output (C0CKO) enable.

0: Disable PCA0 clock output.
1: Enable PCA0 clock output with PCA0 base timer overflow rate/2.

AUXR8: Auxiliary Register 8

SFR Page = **5 only**
SFR Address = 0xA4 RESET = **11**00-0000

7	6	5	4	3	2	1	0
POE7	POE6	C0PPS2	--	KBI0PS0	S1COPS	--	--
R/W	**R/W**	**R/W**	**W**	**R/W**	**R/W**	**W**	**W**

Bit 7: POE7, PCA0 PWM7 main channel (PWM7O) output control.
0: Disable PWM7O output on port pin.
1: Enable PWM7O output on port pin. **Default is enabled.**

Bit 6: POE6, PCA0 PWM6 main channel (PWM6O) output control.
0: Disable PWM6O output on port pin.
1: Enable PWM6O output on port pin. **Default is enabled.**

Bit 5: C0PPS2, {PWM6, PWM7} Port pin Selection 2.

C0PPS2	PWM6	PWM7
0	P6.0	P6.1
1	P3.0	P3.1

Bit 3: KBI0PS0, KBI0~1 Port pin Selection 0.

KBI0PS	KBI0	KBI1
0	P1.0	P1.1
1	**P4.7**	**P3.3**

Bit 2: S1COPS, S1BRG Clock Output (S1CKO) port pin Selection.

S1COPS	S1CKO
0	P4.7
1	P6.1

AUXR9: Auxiliary Register 9

SFR Page = 6 only
SFR Address = 0xA4 RESET = 0000-0000

7	6	5	4	3	2	1	0
--	--	T1G1	T0G1	C0FDC1	C0FDC0	S1PS1	S1PS0
W	**W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**

Bit 1~0: S1PS1~0, Serial Port 1 pin Selection [1:0].

S1PS1~0	RXD1	TXD1
00	P1.0	P1.1
01	P6.0	P6.1
10	P4.4	P4.5
11	P3.4	P3.5

AUXR10: Auxiliary Register 10

SFR Page = **7 only**

SFR Address = 0xA4 RESET = 0000-0000

7	6	5	4	3	2	1	0
--	--	--	SPIPS0	S0PS1	--	TWICF	PAA
W	**W**	**W**	**R/W**	**R/W**	**W**	**R/W**	**R/W**

Bit 4: SPIPS0, SPI Port pin Selection 0.

SPIPS0	nSS	MOSI	MISO	SPICLK
0	P3.3	P1.5	P1.6	P1.7
1	P1.7	P3.5	P3.4	P3.3

XICFG: External Interrupt Configured Register

SFR Page = **0 only**

SFR Address = **0xC1** RESET = 0000-0000

7	6	5	4	3	2	1	0
INT1IS.1	INT1IS.0	INT0IS.1	INT0IS.0	--	X2FLT	X1FLT	X0FLT
R/W	**R/W**	**R/W**	**R/W**	**W**	**R/W**	**R/W**	**R/W**

Bit 7~6: INT1IS.1~0, nINT1 input port pin selection bits which function is defined with INT1IS.2 as following table.

INT1IS.2~0	Selected Port Pin of nINT1
000	P3.3
001	P3.1
010	P3.5
011	P1.0
100	P6.1
101	P3.4
110	P1.5
111	P2.4

Bit 5~4: INT0IS.1~0, nINT0 input port pin selection bits which function is defined with INT0IS.2 as following table.

INT0IS.2~0	Selected Port Pin of nINT0
000	P4.5
001	P3.0
010	P3.4
011	P4.7
100	P6.0
101	P1.1
110	P1.7
111	P2.2

XICFG1: External Interrupt Configured 1 Register

SFR Page = **1 only**

SFR Address = **0xC1** RESET = 0000-0000

7	6	5	4	3	2	1	0
INT1IS.2	INT0IS.2	INT2IS.1	INT2IS.0	--	X2FLT1	X1FLT1	X0FLT1
R/W	**R/W**	**R/W**	**R/W**	**W**	**R/W**	**R/W**	**R/W**

Bit 7: INT1IS2, nINT1 input port pin selection bit which function is defined with INT1IS.1~0.

Bit 6: INT0IS2, nINT0 input port pin selection bit which function is defined with INT0IS.1~0.

Bit 5~4: INT2IS1~0, nINT2 input port pin selection bits which function is defined as following table.

INT2IS.1~0	Selected Port Pin of nINT2
00	P4.4
01	P3.0
10	P1.1
11	P1.6

5. Electrical Characteristics

5.1. Absolute Maximum Rating

Parameter	Rating	Unit
Ambient temperature under bias	-40 ~ +105	°C
Storage temperature	-65 ~ + 150	°C
Voltage on any Port I/O Pin or RST with respect to VSS	-0.5 ~ VDD + 0.5	V
Voltage on VDD with respect to VSS	-0.5 ~ +6.0	V
Maximum total current through VDD and VSS	200	mA
Maximum output current sunk by any Port pin	40	mA

*Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.2. DC Characteristics

VDD = 5.0V±10%, VSS = 0V, T_A = 25 °C and execute NOP for each machine cycle, unless otherwise specified

Symbol	Parameter	Test Condition	Limits			Unit
			min	typ	max	
Input/ Output Characteristics						
V_{IH1}	Input High voltage (All I/O Ports)	Except P6.0, P6.1	0.6			VDD
V_{IH2}	Input High voltage (RST, P6.0, P6.1)		0.75			VDD
V_{IL1}	Input Low voltage (All I/O Ports)	Except P6.0, P6.1			0.15	VDD
V_{IL2}	Input Low voltage (RST, P6.0, P6.1)				0.2	VDD
I_{IH}	Input High Leakage current (All I/O Ports)	V_{PIN} = VDD		0	±1	uA
I_{IL1}	Logic 0 input current (P3 in quasi-mode)	V_{PIN} = 0.4V		-20	-30	uA
I_{IL2}	Logic 0 input current (All Input only or open-drain Ports)	V_{PIN} = 0.4V		0	-1	uA
I_{H2L}	Logic 1 to 0 input transition current (P3 in quasi-mode) (2)	V_{PIN} =1.8V		-300	-450	uA
I_{OH1}	Output High current (P3 in quasi-Mode)	VDD=5V; V_{PIN} =2.4V	-180	-260		uA
		VDD=3.3V; V_{PIN} =2.4V	-50	-80		uA
		VDD=1.8V; V_{PIN} =1.4V	-10	-15		uA
I_{OH2}	Output High current (All push-pull output ports)	VDD=5V; V_{PIN} =2.4V	-25	-34		mA
		VDD=3.3V; V_{PIN} =2.4V	-8	-11		mA
		VDD=1.8V; V_{PIN} =1.4V	-2	-2.6		mA
I_{OH3}	Output High current (All push-pull output ports on low driving strength, except RST Pin)	VDD=5V; V_{PIN} =2.4V	-8	-13.6		mA
		VDD=3.3V; V_{PIN} =2.4V	-3	-4.6		mA
		VDD=1.8V; V_{PIN} =1.4V	0.7	-1.1		mA
I_{OL1}	Output Low current (All I/O Ports)	VDD=5V; V_{PIN} =0.4V	18	24		mA
		VDD=3.3V; V_{PIN} =0.4V	14	17		mA
		VDD=1.8V; V_{PIN} =0.4V	6	8		mA
I_{OL1}	Output Low current (All push-pull output ports on low driving strength, except RST Pin)	VDD=5V; V_{PIN} =0.4V	1.8	3.1		mA
		VDD=3.3V; V_{PIN} =0.4V	1.2	2.2		mA
		VDD=1.8V; V_{PIN} =0.4V	0.55	1.1		mA
R_{RST}	Internal reset pull-down resistance	VDD=5V		125		Kohm
		VDD=3.3V		207		Kohm
		VDD=2.1V		396		Kohm
Power Consumption						
I_{OP1}	Normal mode operating current	SYSCLK = 32MHz @ IHRCO with PLL		6.5		mA
I_{OP2}		SYSCLK = 24MHz @ IHRCO with PLL		5.7		mA
I_{OP3}		SYSCLK = 12MHz @ IHRCO		3.3		mA
I_{OP4}		SYSCLK = 12MHz @ IHRCO, VDD = 5V with ADC 400K sps		5.8		mA
I_{OP5}		SYSCLK = 12MHz @ IHRCO, VDD = 3.3V with ADC 400K sps		5.3		mA
I_{OP6}		SYSCLK = 24MHz @ IHRCO with PLL, VDD = 5V with ADC 800K sps		8.3		mA
I_{OPS1}	Slow mode operating current	SYSCLK = 12MHz/128 @ IHRCO		0.6		mA
I_{IDLE1}	Idle mode operating current	SYSCLK = 12MHz @ IHRCO		1.1		mA
I_{IDLE2}		SYSCLK = 12MHz/128 @ IHRCO		0.45		mA
I_{IDLE3}		SYSCLK = 32KHz @ ILRCO		50		uA

I_{SUB1}	Sub-clock mode operating current	SYSCLK = 32KHz @ ILRCO, BOD1 disabled		65		uA
I_{SUB2}		SYSCLK = 32KHz/128 @ ILRCO, BOD1 disabled		60		uA
I_{WAT}	Watch mode operating current	WDT = 32KHz @ ILRCO in PD mode		5		uA
I_{MON1}	Monitor Mode operating current	BOD1 enabled in PD mode		10		uA
I_{RTC1}	RTC Mode operating current	RTC operating in PD mode, VDD = 5.0V		4.5		uA
I_{PD1}	Power down mode current			2.5		uA
BOD0/BOD1 Characteristics						
V_{BOD0}	BOD0 detection level	T_A = -40°C to +105°C		1.7		V
V_{BOD10}	BOD1 detection level for 2.0V	T_A = -40°C to +105°C		2.0		V
V_{BOD10}	BOD1 detection level for 2.4V	T_A = -40°C to +105°C		2.37		V
V_{BOD11}	BOD1 detection level for 3.7V	T_A = -40°C to +105°C		3.7		V
V_{BOD11}	BOD1 detection level for 4.2V	T_A = -40°C to +105°C		4.2		V
I_{BOD1}	BOD1 Power Consumption	T_A = +25°C, VDD=5.0V		6.5		uA
		T_A = +25°C, VDD=3.3V		5		
Operating Condition						
V_{PSR}	Power-on Slop Rate	T_A = -40°C to +85°C	0.05			V/ms
V_{POR1}	Power-on Reset Valid Voltage	T_A = -40°C to +85°C			0.1	V
V_{OP1}	CPU Operating Speed 0-36MHz	T_A = -40°C to +105°C	2.7		5.5	V
V_{OP2}	CPU Operating Speed 0-24MHz	T_A = -40°C to +105°C	2.2		5.5	V
V_{OP3}	CPU Operating Speed 0-12MHz	T_A = -40°C to +105°C	1.8		5.5	V

(1) Data based on characterization results, not tested in production.

(2) I/O under Quasi-Bidirectional mode, when input voltage High transfer to Low and across the threshold voltage, the internal “Weak” pull up will be turn off. I_{H2L} indicates the current near the threshold voltage.

(3) All current flowing into the chip has a positive value, and current flowing out of the chip has negative value.

5.3. IHRCO Characteristics

Parameter	Test Condition	Limits			Unit
		min	typ	max	
Supply Voltage		1.8		5.5	V
IHRCO Frequency	T_A = +25°C, AFS = 0		12		MHz
	T_A = +25°C, AFS = 1		11.059		MHz
IHRCO Frequency Deviation (factory calibrated)	TA = +25˚C	-1.0		+1.0	%
	TA = -40˚C to +105˚C	-2.0(1)		+2.0(1)	%
IHRCO Start-up Time	TA = -40˚C to +105˚C			32(1)	us
IHRCO Power Consumption	TA = +25˚C, VDD=5.0V		350 (1)		uA

(1) Data based on characterization results, not tested in production.

5.4. ILRCO Characteristics

Parameter	Test Condition	Limits			Unit
		min	typ	max	
Supply Voltage		1.8		5.5	V
ILRCO Frequency	TA = +25˚C		32		KHz
ILRCO Frequency Deviation	TA = +25˚C	-8(1)		+8(1)	%
	TA = -40˚C to +105˚C	-20(1)		+20(1)	%

(1) Data based on characterization results, not tested in production.

5.5. CKM Characteristics

Parameter	Test Condition	Limits			Unit
		min	typ	max	
Supply Voltage	TA = -40˚C to +105˚C	2.2		5.5	V
Clock Input Range	TA = -40˚C to +105˚C	4.5(1)		6.5(1)	MHz
CKM Start-up Time	TA = -40˚C to +105˚C	30(2)		100(2)	us
CKM Power Consumption	TA = +25˚C, VDD=5.0V, CKM = 96MHz		350		uA
	TA = +25˚C, VDD=5.0V, CKM = 144MHz		450		

(1) Data guaranteed by design, not tested in production.
(2) Data based on characterization results, not tested in production.

5.6. Flash Characteristics

Parameter	Test Condition	Limits			Unit
		min	typ	max	
Supply Voltage	TA = -40˚C to +105˚C	1.8		5.5	V
Flash Write (Erase/Program) Voltage	TA = -40˚C to +105˚C	1.8		5.5	V
Flash Erase/Program Cycle	TA = -40˚C to +105˚C	20,000			times
Flash Data Retention	TA = +25˚C	100			year

5.7. ADC Characteristics

VDD=5.0V, T_A= -40°C ~ +85°C unless otherwise specified

Parameter	Test Condition	Limits			Unit
		min	typ	max	
Supply Range					
Supply Voltage		2.4		5.5	V
DC Accuracy					
Resolution			12		bits
Integral Nonlinearity	VDD ≥ 4 V, 800K sps	-3.5		+3.5	LSB
	VDD = 2.4V~5.5V, 400K sps	-3.2		+3	LSB
Differential Nonlinearity	VDD ≥ 4 V, 800K sps	-3		+3	LSB
	VDD = 2.4V~5.5V, 400K sps	-2		+2	
Offset Error	VDD= 2.4V~5.5V		+6	+10	LSB
Conversion Rate					
SAR Conversion Clock			24		MHz
Conversion Time in SAR Clocks			30		clocks
Conversion Rate	VDDA >=4.0		800		K sps
	VDDA >=2.7		533		
	VDDA >=2.4		400		
Analog Inputs					
V_{ADC} Input Voltage Range	Single Ended (AIN+ – GND)	0		VDD	V
Input Capacitance			9.17	10.58	pF
Input Sampling switch resistance note1	VDD = 5V		714		Ω
	VDD = 4.2V		857		Ω
	VDD = 3.3V		968		Ω
	VDD = 2.7V		1050		Ω
Switch Channel Stable Time					
Switch from VDD to Pulldown R	CH0(VDD)→CH1(51K Pulldown)		4.9		us
	CH0(VDD)→CH1(10K Pulldown)		0.8		
Switch from GND to Pullup R	CH0(GND)→CH1(51K Pullup)		5.2		
	CH0(GND)→CH1(10K Pullup)		1.4		
Switch from VDD to resistor divider (VDD/2)	CH0(VDD)→CH1(VDD/2，51K resistor divider)		4.3		
Switch from VDD to resistor divider (VDD/2)	CH0(GND)→CH1(VDD/2，10K resistor divider)		0.7		
Switch from GND to resistor divider (VDD/2)	CH0(GND)→CH1(VDD/2，51K resistor divider)		4.1		
Switch from GND to resistor divider (VDD/2)	CH0(GND)→CH1(VDD/2，10K resistor divider)		0.6		
Power Consumption					
Power Supply Current	ADPS<1:0>=00	2.3		2.9	mA
	ADPS<1:0>=01	2.2		2.8	
	ADPS<1:0>=10	2.1		2.6	
	ADPS<1:0>=11	2		2.5	

Note1: Data guaranteed by design, not tested in production.

5.8. IVR Characteristics

VDD=5.0V±10%, VSS=0V, T_A =-40°C to +105°C, C_{LOAD}=4.7upF/0.1ohm-ESR unless otherwise specified

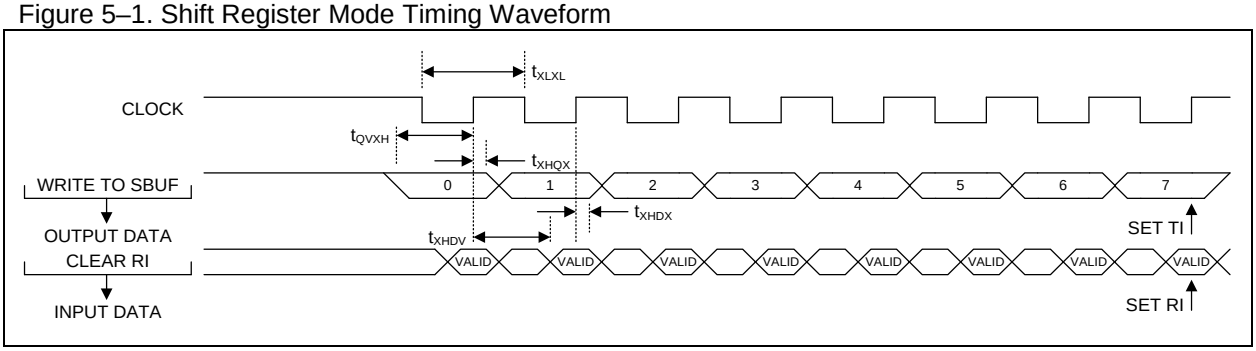
Parameter	Test Condition	Limits			Unit
		Min.	Typ.	Max.	
Supply Range					
Supply Voltage		2.4	5.0	5.5	V
Operation Current	Normal Power State	43		67	uA
	Low Power State		0.1		uA
DC Accuracy					
Output Supply Voltage	-40°C ~ +85°C	1.37	1.4	1.43	V
Spread over the temperature range	VDD = 3.3V±10mV			13	mV

5.9. Serial Port Timing Characteristics

VDD = 5.0V±10%, VSS = 0V, T_A = -40°C to +105°C, unless otherwise specified

Symbol	Parameter	URM0X3 = 0		URM0X3 = 1		Unit
		Min.	Max	Min.	Max	
t_{XLXL}	Serial Port Clock Cycle Time	12T		4T		T_{SYSCLK}
t_{QVXH}	Output Data Setup to Clock Rising Edge	10T-20		2T-20		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	T-10		T-10		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	5		5		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		2T-10		2T-10	ns

Figure 5–1. Shift Register Mode Timing Waveform



5.10. SPI Timing Characteristics

VDD = 5.0V±10%, VSS = 0V, T_A = -40°C to +105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Units
Master Mode Timing				
t_{MCKH}	SPICLK High Time	1T		T_{SYSCLK}
t_{MCKL}	SPICLK Low Time	1T		T_{SYSCLK}
t_{MIS}	MISO Valid to SPICLK Sample Edge	10		ns
t_{MIH}	SPICLK Shift Edge to MISO Change	0		ns
t_{MOH}	SPICLK Shift Edge to MOSI Change		10	ns
Slave Mode Timing				
t_{SE}	nSS Falling to First SPICLK Edge	2T		T_{SYSCLK}
t_{SD}	Last SPICLK Edge to nSS Rising	2T		T_{SYSCLK}
t_{SEZ}	nSS Falling to MISO Valid		4T	T_{SYSCLK}
t_{SDZ}	nSS Rising to MISO High-Z		4T	T_{SYSCLK}
t_{CKH}	SPICLK High Time	2T		T_{SYSCLK}
t_{CKL}	SPICLK Low Time	2T		T_{SYSCLK}
t_{SIS}	MOSI Valid to SPICLK Sample Edge	1T		T_{SYSCLK}
t_{SIH}	SPICLK Sample Edge to MOSI Change	1T		T_{SYSCLK}
t_{SOH}	SPICLK Shift Edge to MISO Change		2T	T_{SYSCLK}
t_{SLH}	Last SPICLK Edge to MISO Change (CPHA = 1 ONLY)	1T	2T	T_{SYSCLK}

Figure 5–2. SPI Master Transfer Waveform with CPHA=0

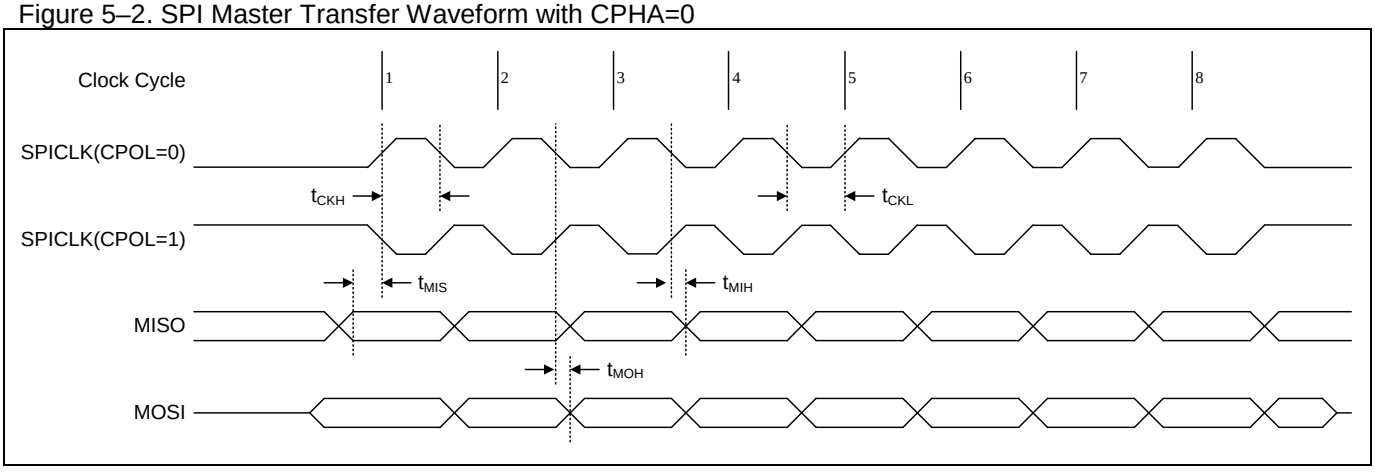


Figure 5–3. SPI Master Transfer Waveform with CPHA=1

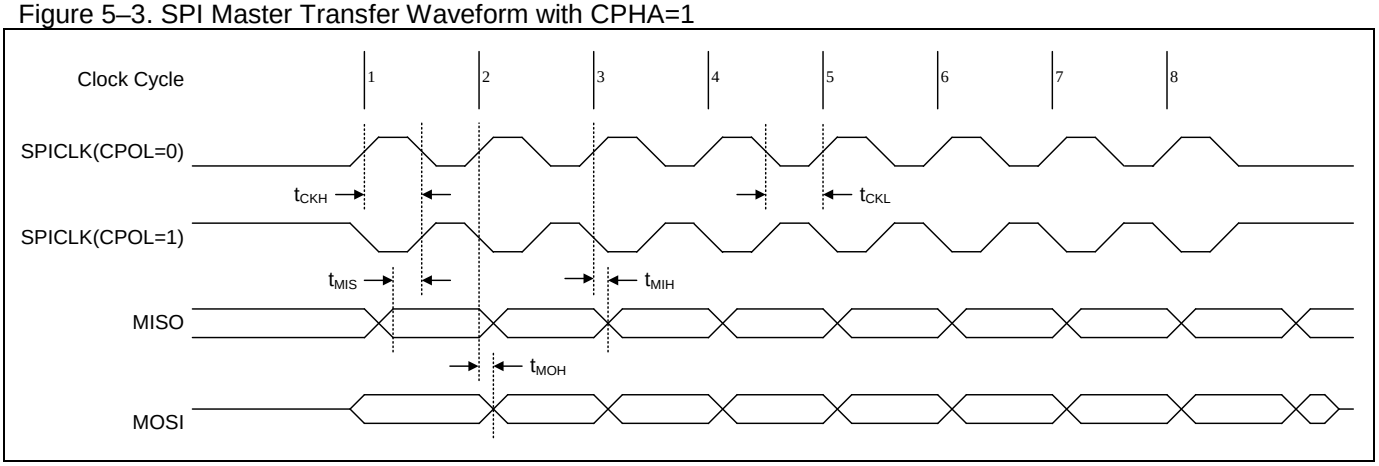


Figure 5–4. SPI Slave Transfer Waveform with CPHA=0

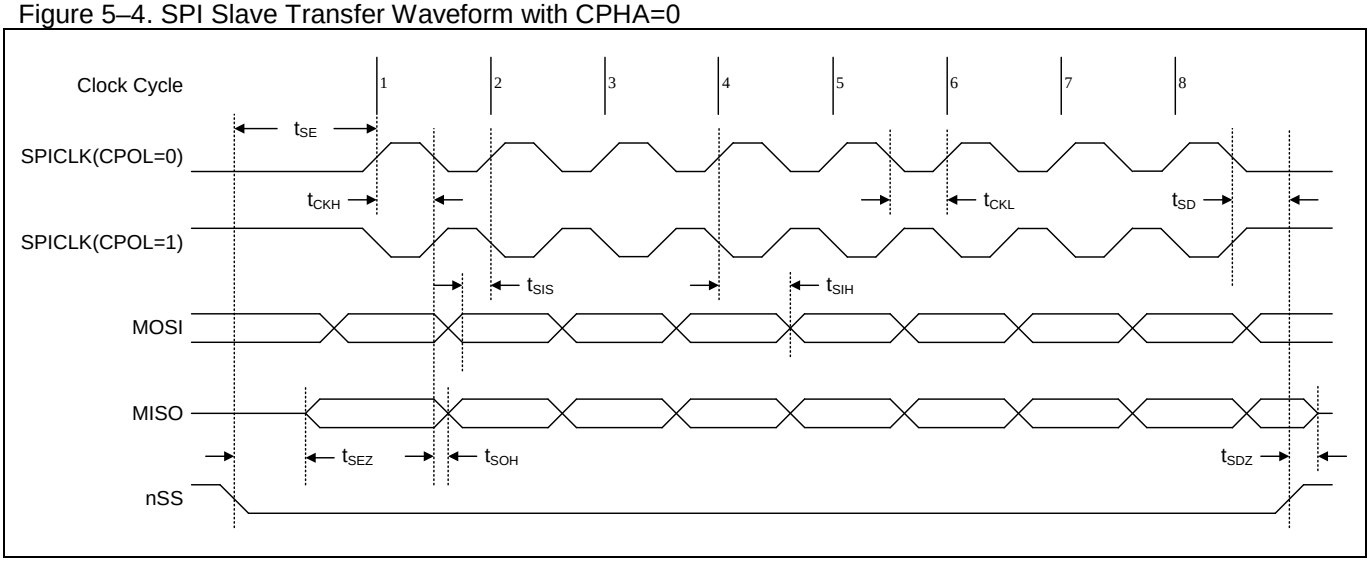
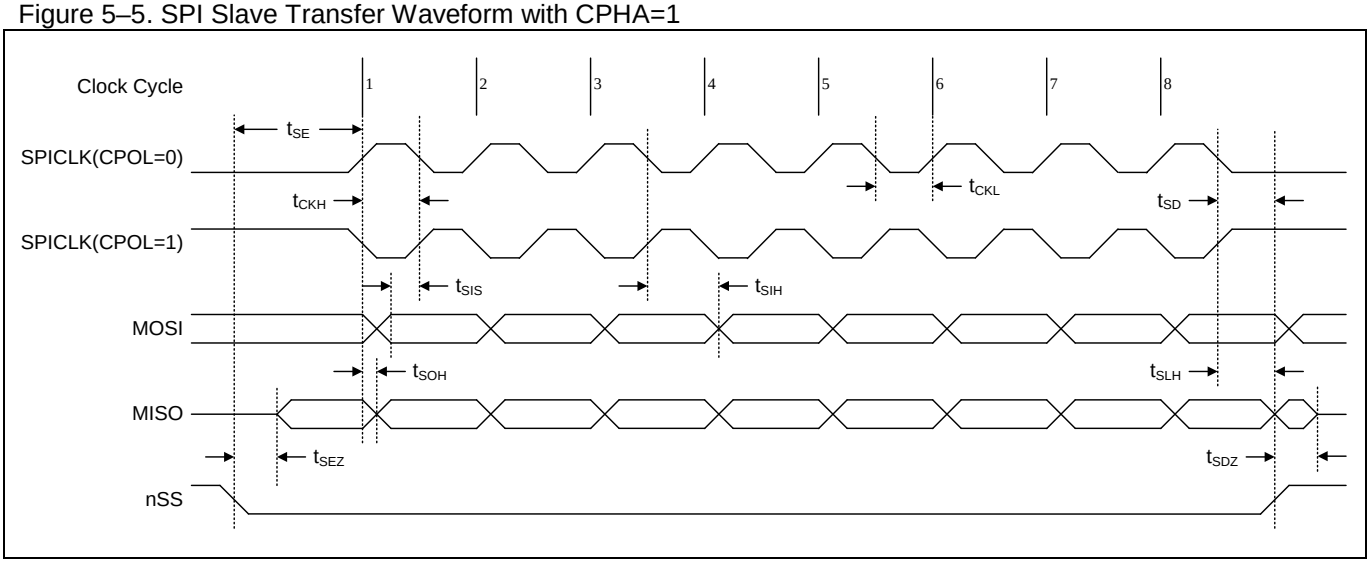


Figure 5–5. SPI Slave Transfer Waveform with CPHA=1



6. Instruction Set

Table 6–1. Instruction Set

MNEMONIC	DESCRIPTION	BYTE	EXECUTION Cycles
DATA TRASFER			
MOV A,Rn	Move register to Acc	1	1
MOV A,direct	Move direct byte o Acc	2	2
MOV A,@Ri	Move indirect RAM to Acc	1	2
MOV A,#data	Move immediate data to Acc	2	2
MOV Rn,A	Move Acc to register	1	2
MOV Rn,direct	Move direct byte to register	2	4
MOV Rn,#data	Move immediate data to register	2	2
MOV direct,A	Move Acc to direct byte	2	3
MOV direct,Rn	Move register to direct byte	2	3
MOV direct,direct	Move direct byte to direct byte	3	4
MOV direct,@Ri	Move indirect RAM to direct byte	2	4
MOV direct,#data	Move immediate data to direct byte	3	3
MOV @Ri,A	Move Acc to indirect RAM	1	3
MOV @Ri,direct	Move direct byte to indirect RAM	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	2	3
MOV DPTR,#data16	Load DPTR with a 16-bit constant	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to Acc	1	4
MOVC A,@A+PC	Move code byte relative to PC to Acc	1	4
MOVX A,@Ri	Move on-chip auxiliary RAM(8-bit address) to Acc	1	3
MOVX A,@DPTR	Move on-chip auxiliary RAM(16-bit address) to Acc	1	3
MOVX @Ri,A	Move Acc to on-chip auxiliary RAM(8-bit address)	1	3
MOVX @DPTR,A	Move Acc to on-chip auxiliary RAM(16-bit address)	1	3
MOVX A,@Ri	Move external RAM(8-bit address) to Acc	1	not support
MOVX A,@DPTR	Move external RAM(16-bit address) to Acc	1	not support
MOVX @Ri,A	Move Acc to external RAM(8-bit address)	1	not support
MOVX @DPTR,A	Move Acc to external RAM(16-bit address)	1	not support
PUSH direct	Push direct byte onto Stack	2	4
POP direct	Pop direct byte from Stack	2	3
XCH A,Rn	Exchange register with Acc	1	3
XCH A,direct	Exchange direct byte with Acc	2	4
XCH A,@Ri	Exchange indirect RAM with Acc	1	4
XCHD A,@Ri	Exchange low-order digit indirect RAM with Acc	1	4
ARITHEMATIC OPERATIONS			
ADD A,Rn	Add register to Acc	1	2
ADD A,direct	Add direct byte to Acc	2	3
ADD A,@Ri	Add indirect RAM to Acc	1	3
ADD A,#data	Add immediate data to Acc	2	2
ADDC A,Rn	Add register to Acc with Carry	1	2
ADDC A,direct	Add direct byte to Acc with Carry	2	3
ADDC A,@Ri	Add indirect RAM to Acc with Carry	1	3
ADDC A,#data	Add immediate data to Acc with Carry	2	2
SUBB A,Rn	Subtract register from Acc with borrow	1	2
SUBB A,direct	Subtract direct byte from Acc with borrow	2	3
SUBB A,@Ri	Subtract indirect RAM from Acc with borrow	1	3

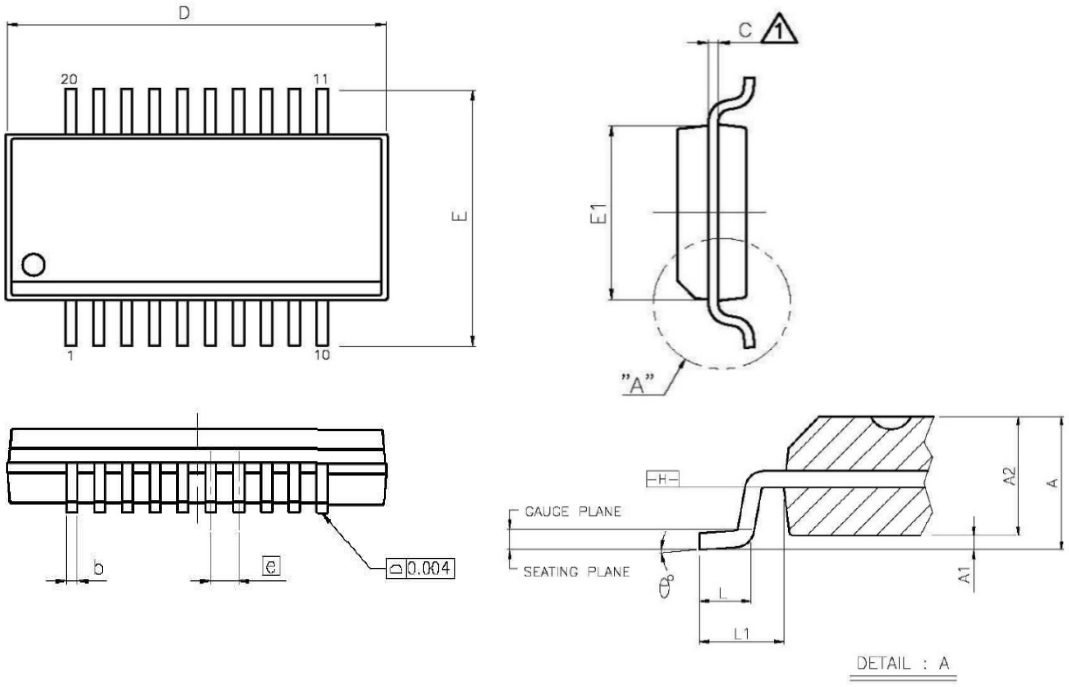
MNEMONIC	DESCRIPTION	BYTE	EXECUTION Cycles
SUBB A,#data	Subtract immediate data from Acc with borrow	2	2
INC A	Increment Acc	1	2
INC Rn	Increment register	1	3
INC direct	Increment direct byte	2	4
INC @Ri	Increment indirect RAM	1	4
DEC A	Decrement Acc	1	2
DEC Rn	Decrement register	1	3
DEC direct	Decrement direct byte	2	4
DEC @Ri	Decrement indirect RAM	1	4
INC DPTR	Increment DPTR	1	1
MUL AB	Multiply A and B	1	4
DIV AB	Divide A by B	1	5
DA A	Decimal Adjust Acc	1	4
LOGIC OPERATION			
ANL A,Rn	AND register to Acc	1	2
ANL A,direct	AND direct byte to Acc	2	3
ANL A,@Ri	AND indirect RAM to Acc	1	3
ANL A,#data	AND immediate data to Acc	2	2
ANL direct,A	AND Acc to direct byte	2	4
ANL direct,#data	AND immediate data to direct byte	3	4
ORL A,Rn	OR register to Acc	1	2
ORL A,direct	OR direct byte to Acc	2	3
ORL A,@Ri	OR indirect RAM to Acc	1	3
ORL A,#data	OR immediate data to Acc	2	2
ORL direct,A	OR Acc to direct byte	2	4
ORL direct,#data	OR immediate data to direct byte	3	4
XRL A,Rn	Exclusive-OR register to Acc	1	2
XRL A,direct	Exclusive-OR direct byte to Acc	2	3
XRL A,@Ri	Exclusive-OR indirect RAM to Acc	1	3
XRL A,#data	Exclusive-OR immediate data to Acc	2	2
XRL direct,A	Exclusive-OR Acc to direct byte	2	4
XRL direct,#data	Exclusive-OR immediate data to direct byte	3	4
CLR A	Clear Acc	1	1
CPL A	Complement Acc	1	2
RL A	Rotate Acc Left	1	1
RLC A	Rotate Acc Left through the Carry	1	1
RR A	Rotate Acc Right	1	1
RRC A	Rotate Acc Right through the Carry	1	1
SWAP A	Swap nibbles within the Acc	1	1
BOOLEAN VARIABLE MANIPULATION			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	4
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	4
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	4
ANL C,bit	AND direct bit to Carry	2	3

MNEMONIC	DESCRIPTION	BYTE	EXECUTION Cycles
ANL C,/bit	AND complement of direct bit to Carry	2	3
ORL C,bit	OR direct bit to Carry	2	3
ORL C,/bit	OR complement of direct bit to Carry	2	3
MOV C,bit	Move direct bit to Carry	2	3
MOV bit,C	Move Carry to direct bit	2	4
BOOLEAN VARIABLE MANIPULATION			
JC rel	Jump if Carry is set	2	3
JNC rel	Jump if Carry not set	2	3
JB bit,rel	Jump if direct bit is set	3	4
JNB bit,rel	Jump if direct bit not set	3	4
JBC bit,rel	Jump if direct bit is set and then clear bit	3	5
PROAGRAM BRACHING			
ACALL addr11	Absolute subroutine call	2	6
LCALL addr16	Long subroutine call	3	6
RET	Return from subroutine	1	4
RETI	Return from interrupt subroutine	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if Acc is zero	2	3
JNZ rel	Jump if Acc not zero	2	3
CJNE A,direct,rel	Compare direct byte to Acc and jump if not equal	3	5
CJNE A,#data,rel	Compare immediate data to Acc and jump if not equal	3	4
CJNE Rn,#data,rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri,#data,rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn,rel	Decrement register and jump if not equal	2	4
DJNZ direct,rel	Decrement direct byte and jump if not equal	3	5
NOP	No Operation	1	1

7. Package Dimension

7.1. SSOP-20(150 mil) Dimension

Figure 7-1. SSOP-20 (150 mil) Package Dimension

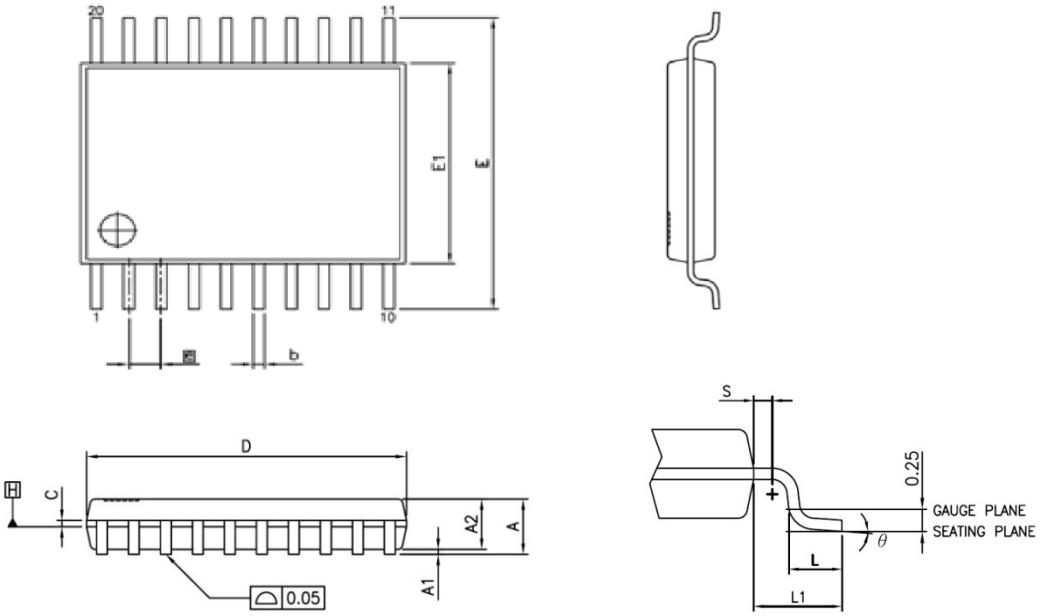


Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.346	1.625	1.752	0.053	0.064	0.069
A1	0.101	0.152	0.254	0.004	0.006	0.010
A2	----	----	1.498	----	----	0.059
b	0.203	----	0.304	0.008	----	0.012
C	0.177	----	0.254	0.007	----	0.010
D	8.559	8.661	8.737	0.337	0.341	0.344
E	5.791	5.994	6.197	0.228	0.236	0.244
E1	3.810	3.911	3.987	0.150	0.154	0.157
e	0.635 BASIC			0.025 BASIC		
L	0.406	0.635	1.270	0.016	0.025	0.050
L1	1.041 BASIC			0.040 BASIC		
θ	0°	----	8°	0°	----	8°

7.2. TSSOP-20(173 mil) Dimension

Figure 7-2. TSSOP-20 6.5 x 4.4mm, 0.65mm pitch Package Dimension

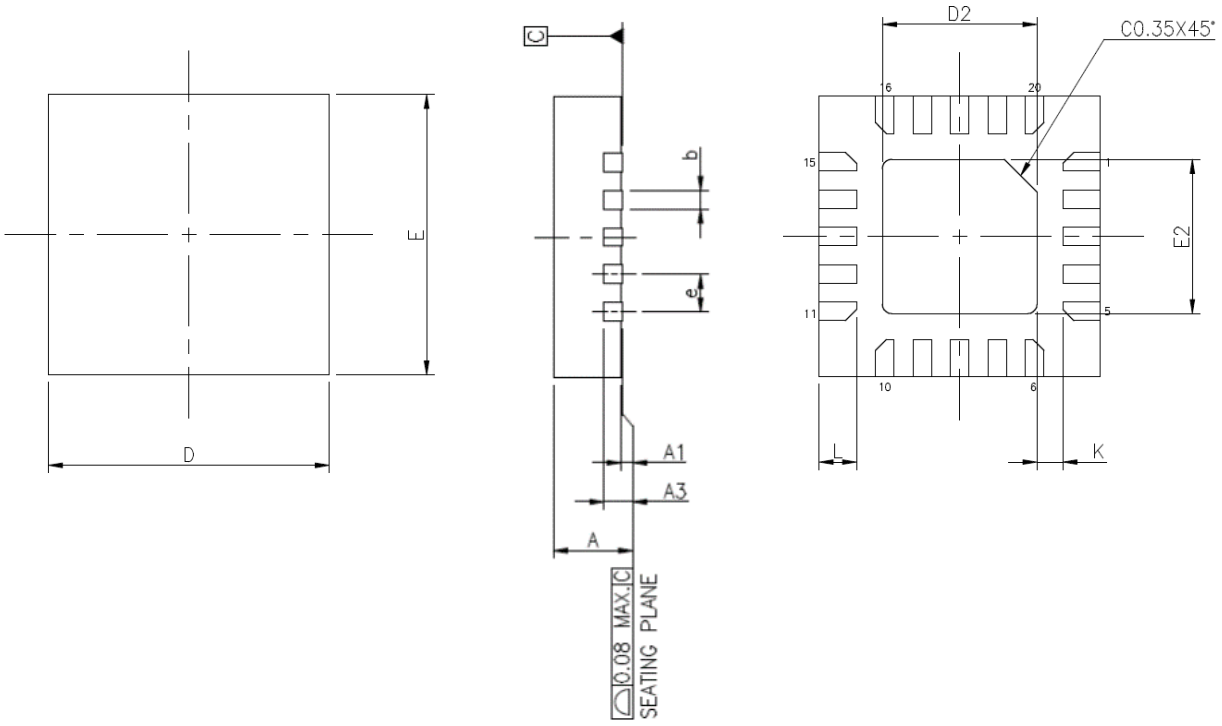
TSSOP-20



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	1.20	----	----	0.047
A1	0.05	----	0.15	0.001	----	0.005
A2	0.80	0.90	1.05	0.031	0.035	0.041
b	0.19	----	0.30	0.007	----	0.011
C	0.09	-----	0.20	0.003	-----	0.007
D	6.40	6.50	6.60	0.251	0.255	0.259
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.40 BSC			0.251 BSC		
e	0.65 BSC			0.025 BSC		
L1	1.00 REF			0.039 REF		
L	0.50	0.60	0.75	0.019	0.023	0.029
S	0.20	----	----	0.007	----	----
θ	0°	----	8°	0°	----	8°

7.3. QFN-20 (3x3x0.55mm) Package Dimension

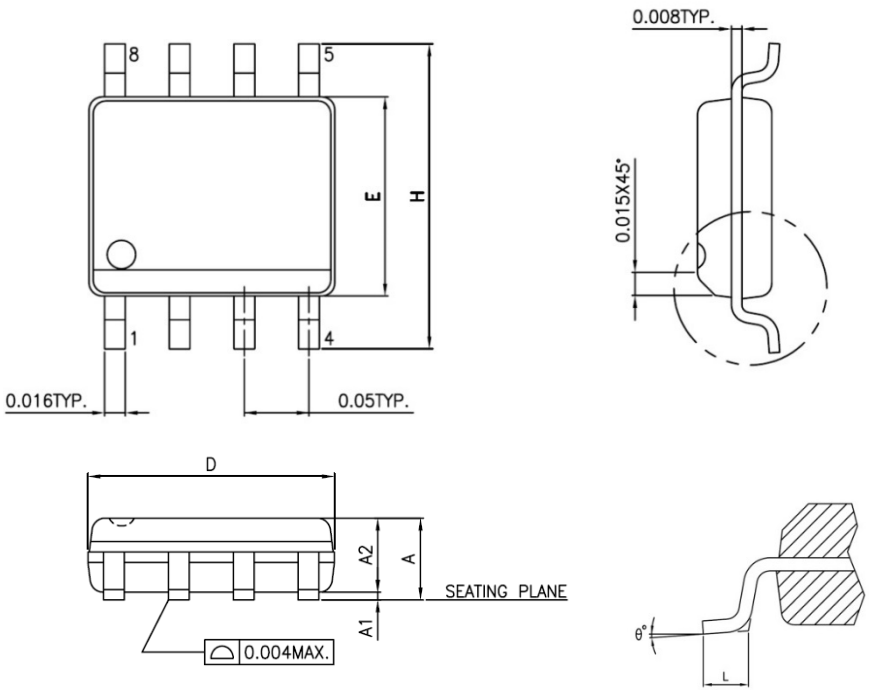
Figure 7-3. QFN-20 (3x3 x 0.55mm) Package Dimension



Unit	mm			inch		
JEDEC	MO-220			MO-220		
PKG	WQFN(X319)			WQFN(X319)		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.50	0.55	0.60	0.019	0.021	0.023
A1	0.00	0.02	0.05	0.000	0.000	0.001
A3	0.150 REF.			0.005 REF.		
b	0.15	0.20	0.25	0.005	0.007	0.009
D	3.00 BSC			0.11 BSC		
E	3.00 BSC			0.11 BSC		
e	0.40 BSC			0.015 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
K	0.20	---	---	0.007	---	---
D2	1.60	1.65	1.70	0.062	0.064	0.066
E2	1.60	1.65	1.70	0.062	0.064	0.066

7.4. SOP-8 (150mil) Package Dimension

Figure 7-4. SOP-8 (150 mil) Package Dimension



Unit	mm		inch	
Symbols	Min.	Max.	Min.	Max.
A	1.346	1.752	0.052	0.068
A1	0.101	0.254	0.003	0.010
A2	1.346	1.498	0.052	0.058
D	4.800	4.978	0.188	0.195
E	3.810	3.987	0.150	0.156
H	5.791	6.197	0.227	0.243
L	0.406	1.270	0.015	0.050
θ	0°	8°	0	8

8. Revision History

Table 8–1. Revision History

Rev	Descriptions	Date
V0.35T	Initial version preliminary released	2019/03/18
V0.36T	1. Modified example of ADC Channel Scan Mode by DMA 2. Add IVR Characteristics 3. Fixed ADCFG0 Bit7~5 table description 4. Modified S0BRG description	2019/04/08
V0.37T	1. Modified ADC DMA description 2. Removed P6FDC, P6DC0 3. Add BME6 description 4. Modified DBSD[1:0] to DBSD 5. Modified CKMI output maximum frequency from 96MHz to 144MHz 6. Modified electrical characteristics 7. Modified ILRCO tolerance 8. Fixed error in SFR table, EPCnH to ECAPnH and EPCnL to ECAPnL 9. Modified HSE, HSE1 description 10. Added description on C0M0 11. Modified STOF, STAF description	2019/05/07
V0.38	1. Added SOP8 Package, and add ICP limitation description for SOP8	2019/09/03
V1.00	1. Modify description of bit SBF0 and TXER0 2. Modify section 32.3 OCD description, to change the PCON3 to DCON0. 3. Removed ADC AZEN description. 4. Modified T2MS0 and T3MS0 table 5. Removed AC0 description in Chapter 27. 6. Added ADCWI, SMPF in ADC interrupt source and CCFn (n=6~7) in PCA0 interrupt source in interrupt Table 15-1 and Table 15-2	2021/3/4

9. Disclaimers

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