NS8002 2.4WMonoABclass audio power amplifier

1characteristic

- Output Power:2. 4W(RL=4Ω,THD=10%) Low leakage
- current in power-down mode:1uA(typical)
- high levelShut-down
- useSOP8encapsulation
- External gain adjustable
- voltage range3.0V—5.25V
- No need to drive output coupling capacitors, bootstrap capacitors, and snubber networks
- Unity Gain Stable

2Application range

- laptop
- Desktop PC
- Low voltage sound system

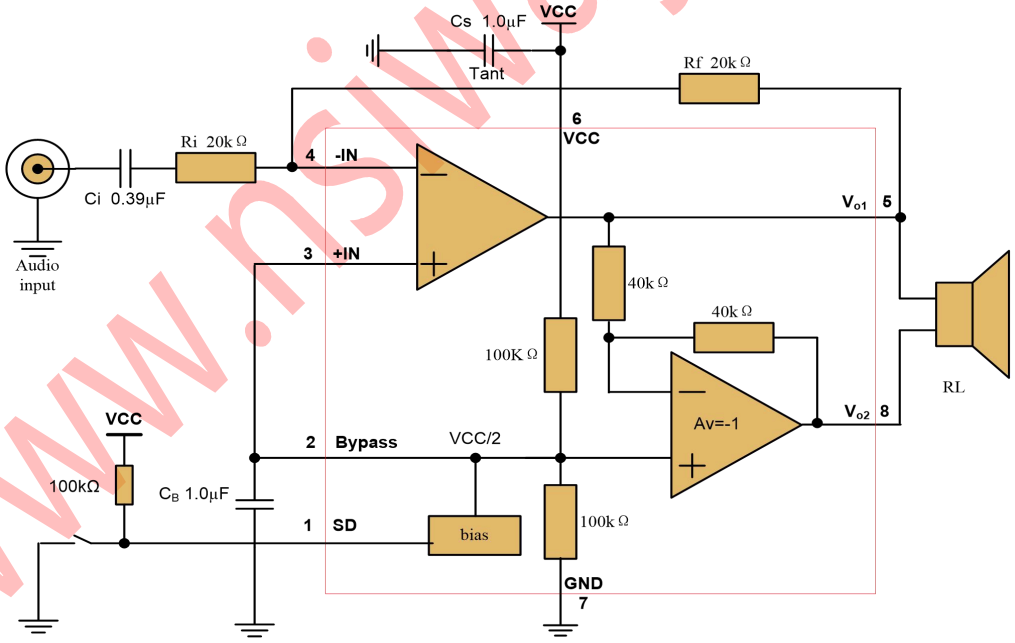
3illustrate

NS8002is aABBridge-like output audio power amplifier. Its application circuit is simple and requires only a few peripheral devices. output not required External coupling capacitors or boost capacitors and buffer networks are required.SOP-8 package, more suitable for portable systems.

NS8002Power consumption can be reduced by controlling entry into a low-power shutdown mode. Gain-bandwidth product up to2.5MHzAnd unity gain stable. The voltage gain of the amplifier can be adjusted by configuring peripheral resistors, which is convenient for application.

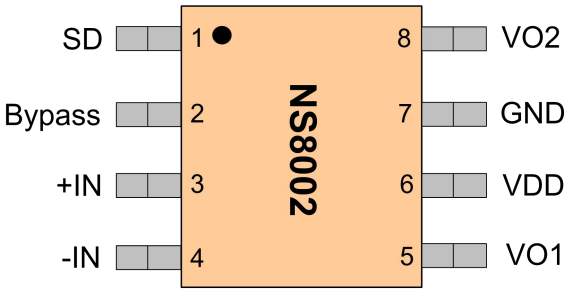
NS8002supplySOP-8package, rated for the operating temperature range of -40°C to85°C.

4Typical Application Circuit



5pin configuration

SOP-8The pinout diagram is shown in the figure below:



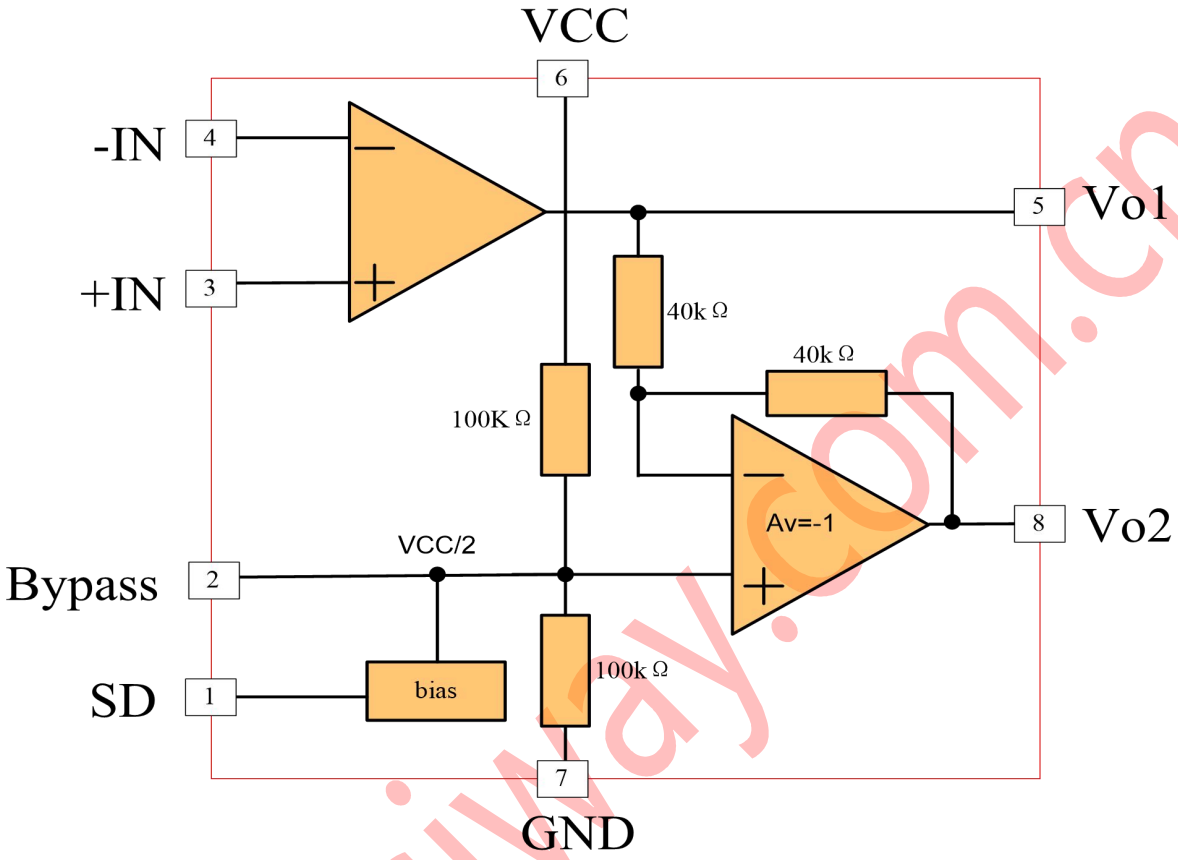
Numbering	Pin name	Pin Description
1	SD	Power-down control pin, high level off, low level on
2	Bypass	Internal Common Mode Voltage Bypass Capacitor
3	+ IN	Analog input, positive phase
4	- IN	Analog input, inverting
5	VO1	Analog output1
6	VDD	Power positive
7	GND	power ground
8	VO2	Analog output2

6Limit working parameters

- Power supply voltage range ..... 2.8V ~ 5.5V
- Input voltage range ..... - 0.3V ~ VDDV
- ESDVoltage(HBM/MM) 3000V/250V
- range of working temperature ..... - 40℃ ~ +85℃
- storage temperature range ..... -65℃ ~ +150℃
- maximum junction temperature ..... + 150℃
- soldering temperature (10sInside) ..... + 220℃
- θ_{JC}/θ_{JA} 35/140oC/W

Note: Exceeding the above limit operating parameter range may cause permanent damage to the chip. Prolonged exposure to any of the above extreme conditions may affect chip reliability and lifetime.

7Structure diagram



8electrical characteristics

Working conditions (unless otherwise stated):T=25℃,VDDB=5.0V.

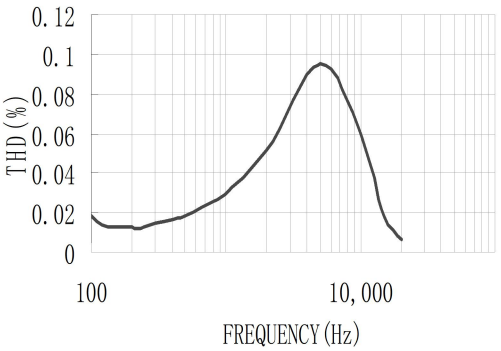
symbol	parameter	Test Conditions	minimum value	standard value	maximum value	unit
VDD	voltage		3.0		5.25	V
IDD	Power Quiescent Current	VIN=0V,Io=0A,		6	10	mA
ISD	OFF Leakage Current			1	20	μA
VOS	Output offset voltage			5.7	50	mV
RO	output resistance		7	8.5	10	K
PO	Output Power	THD=1%, f=1KHz RL=4Ω RL=8Ω		1.8 1.3		W
		THD+N=10%, f=1KHz RL=4Ω RL=8Ω		twenty four 1.7		W
THD+N	Total Distortion + Noise	AVD=2 20Hz≤f≤20KHz RL=4Ω, PO=1W RL=8Ω, PO=0.5W		0.1 0.1		%
PSRR	Power Supply Rejection Ratio		65	80		dB
SNR	SNR	RL=4Ω, Po=1W		85		dB

9Typical characteristic curve

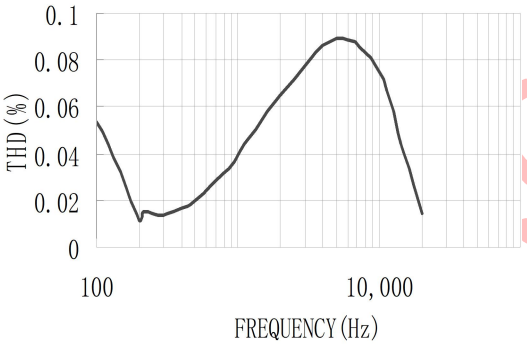
Of the following characteristic curves, unless conditions are specified,T=25℃.

9.1Total Harmonic Distortion (THD), distortion + noise (THD+N), SNR (S/N)

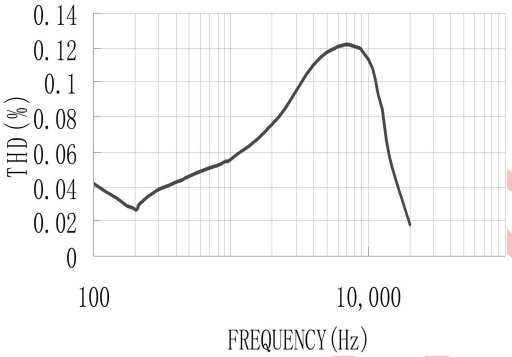
THD vs Frequency
T=25℃, Vdd=5V, RL=8Ω, and Po=500mW



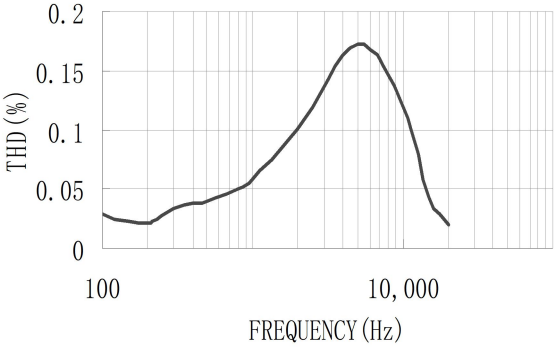
THD vs Frequency
T=25℃, Vdd=3.3V, RL=8Ω, and Po=425mW



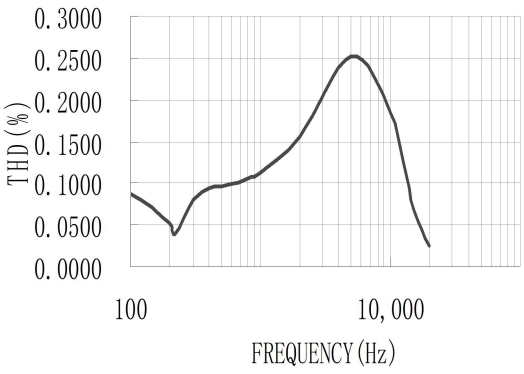
THD vs Frequency
T=25℃, Vdd=2.5V, RL=8Ω, and Po=150mW



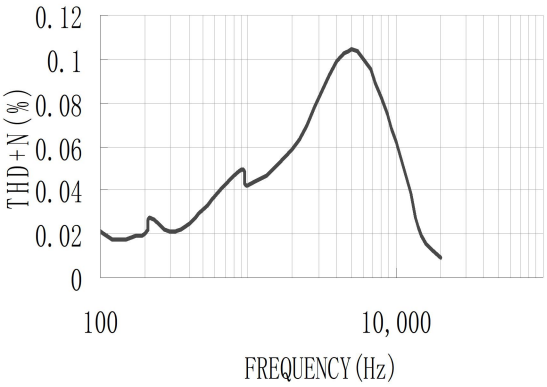
THD vs Frequency
T=25℃, Vdd=3.3V, RL=4Ω, and Po=425mW



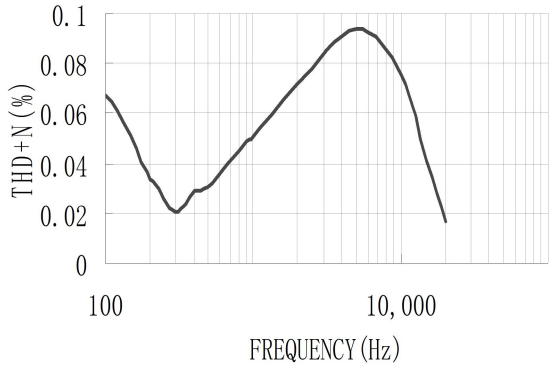
THD vs Frequency
T=25℃, Vdd=2.5V, RL=4Ω, and Po=150mW



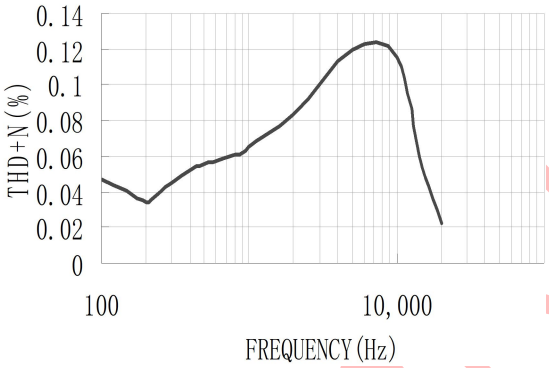
THD+N vs Frequency
T=25℃, Vdd=5V, RL=8Ω, and Po=500mW



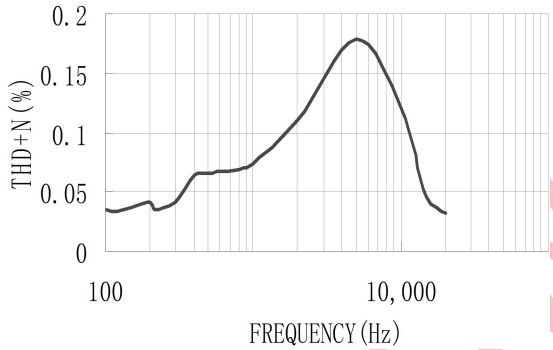
THD+N vs Frequency
T=25℃, Vdd=3.3V, RL=8Ω, and Po=425mW



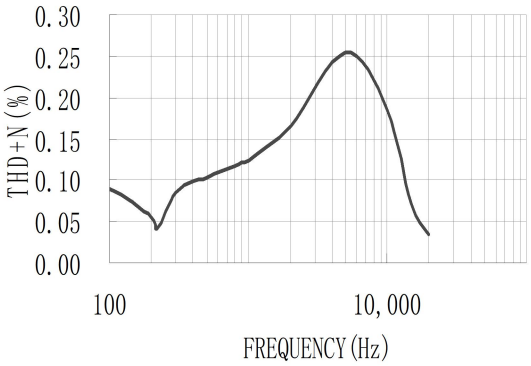
THD+N vs Frequency
T=25℃, Vdd=2.5V, RL=8Ω, and Po=150mW



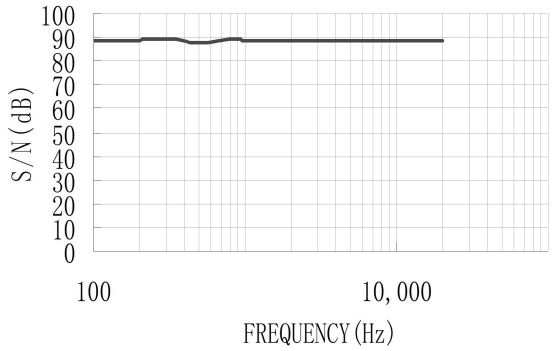
THD+N vs Frequency
T=25℃, Vdd=3.3V, RL=4Ω, and Po=425mW



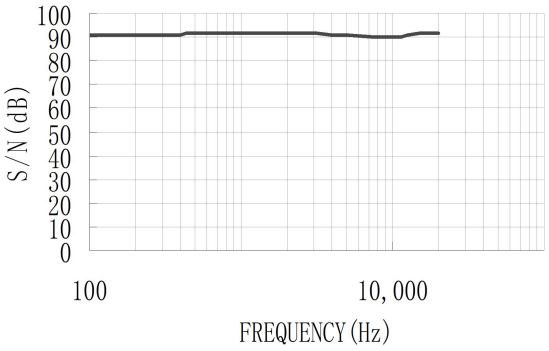
THD+N vs Frequency
T=25℃, Vdd=2.5V, RL=4Ω, and Po=150mW



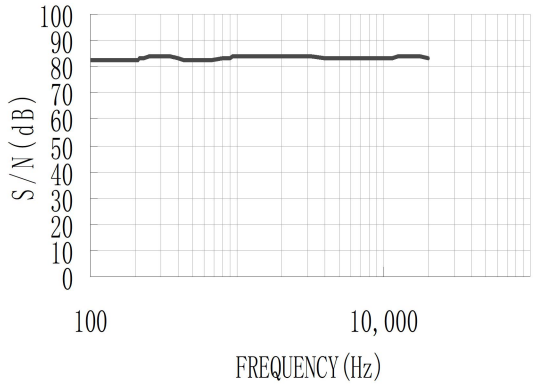
S/N vs Frequency
T=25℃, Vdd=5V, RL=8Ω, and Po=500mW



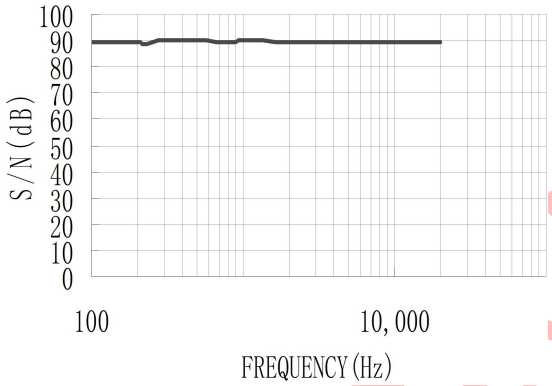
S/N vs Frequency
T=25℃, Vdd=3.3V, RL=8Ω, and Po=425mW



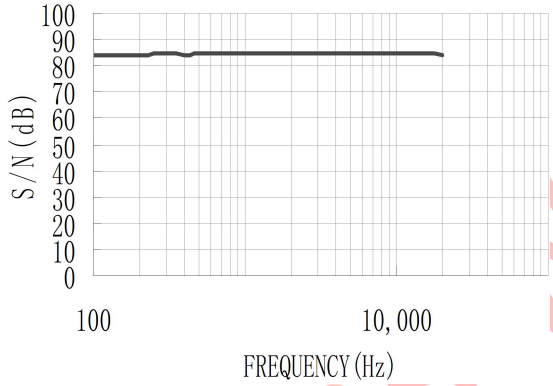
S/N vs Frequency
T=25℃, Vdd=2.5V, RL=8Ω, and Po=150mW



S/N vs Frequency
T=25℃, Vdd=3.3V, RL=4Ω, and Po=425mW

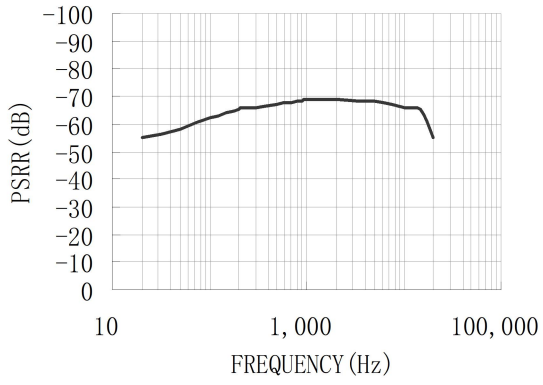


S/N vs Frequency
T=25℃, Vdd=2.5V, RL=4Ω, and Po=150mW

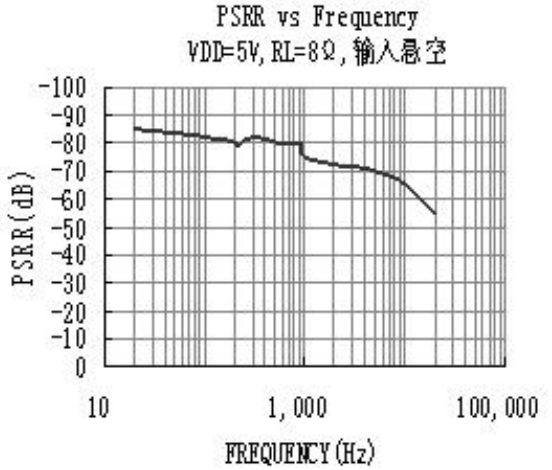


9.2Supply Voltage Rejection Ratio (PSRR)

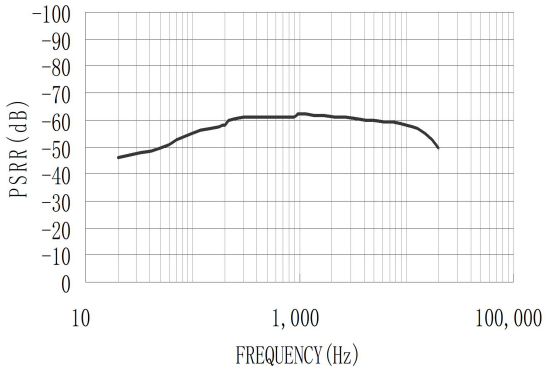
PSRR vs Frequency
VDD=5V, RL=8Ω, 输入接10Ω电阻



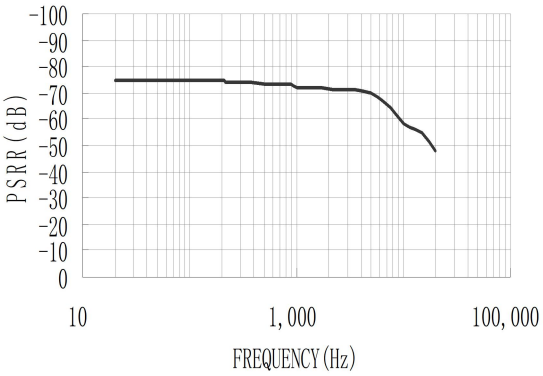
PSRR vs Frequency
VDD=5V, RL=8Ω, 输入悬空



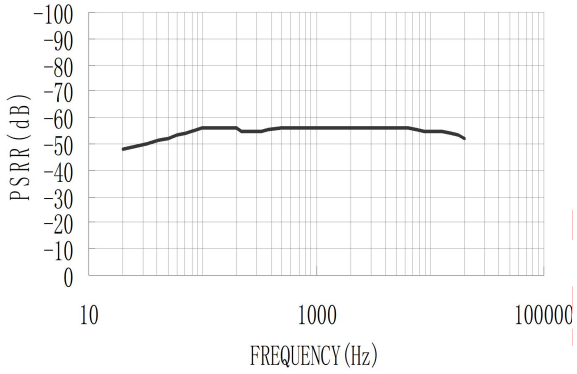
PSRR vs Frequency
VDD=3.3V, RL=8Ω, 输入接10Ω电阻



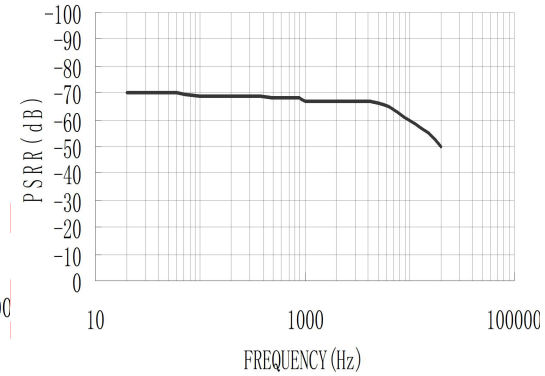
PSRR vs Frequency
VDD=3.3V, RL=8Ω, 输入悬空



PSRR vs Frequency
VDD=2.5V, RL=8Ω, 输入接10Ω电阻

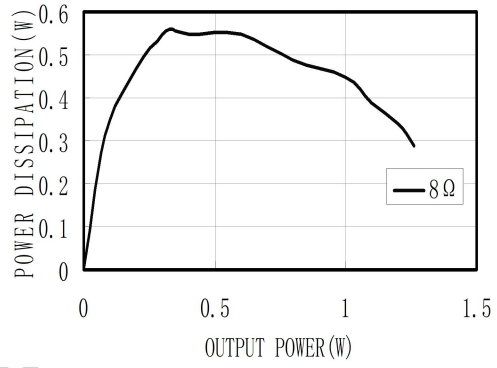


PSRR vs Frequency
VDD=2.5V, RL=8Ω, 输入悬空

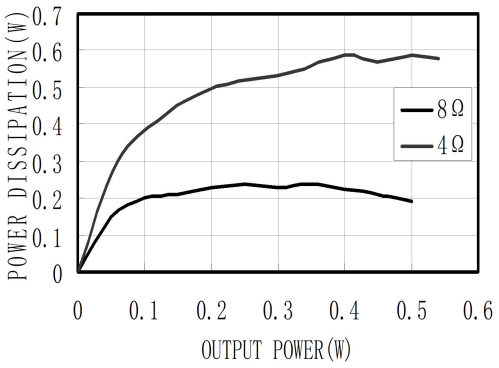


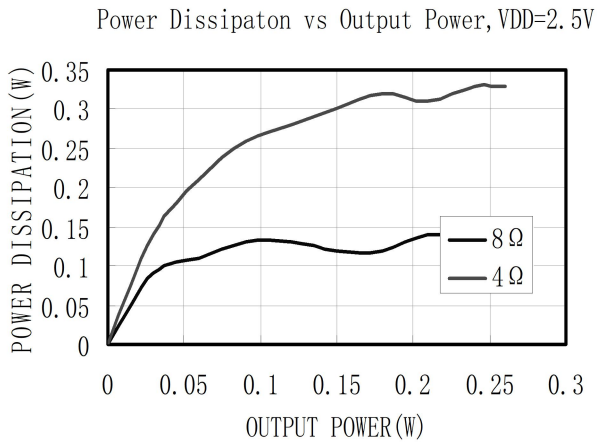
9.3chip power dissipation (Power Dissipation)

Power Dissipaton vs Output Power, VDD=5V

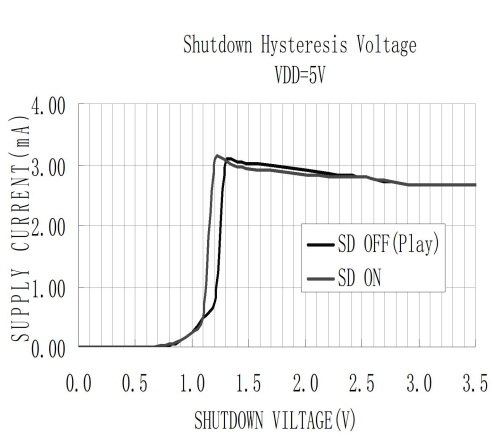


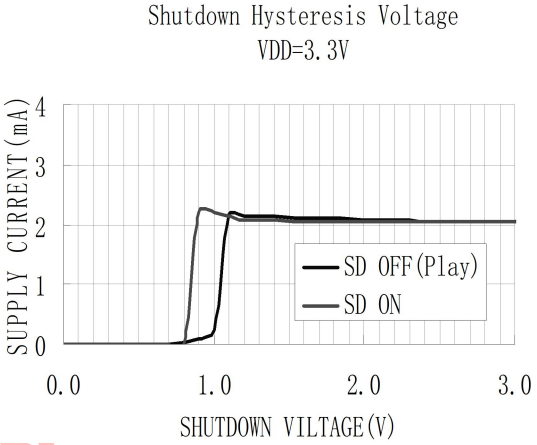
Power Dissipaton vs Output Power, VDD=3.3V

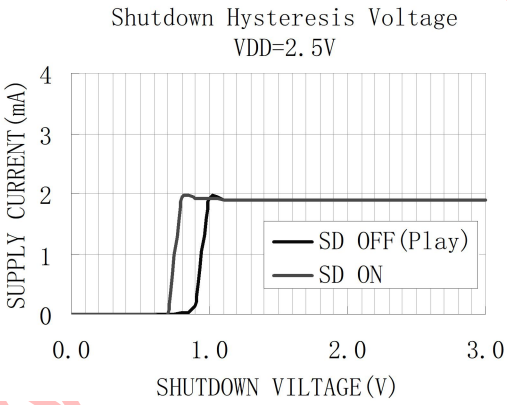




9.4Shutdown hysteresis (Shut Down Hysteresis)

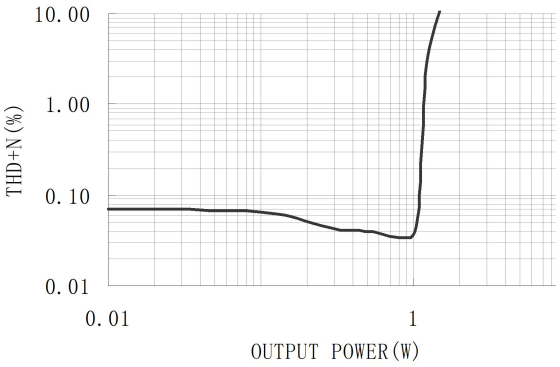




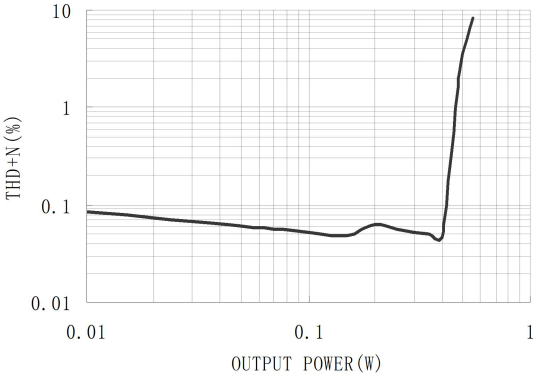


9.5Output Power(Output Power)

THD+N vs OutputPower VDD=5V, RL=8Ω, and f=1KHz

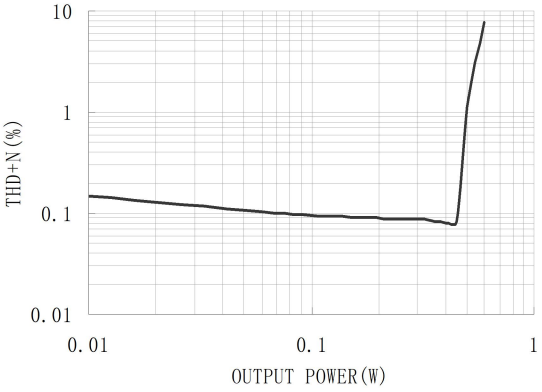


THD+N vs OutputPower VDD=3.3V, RL=8Ω, and f=1KHz

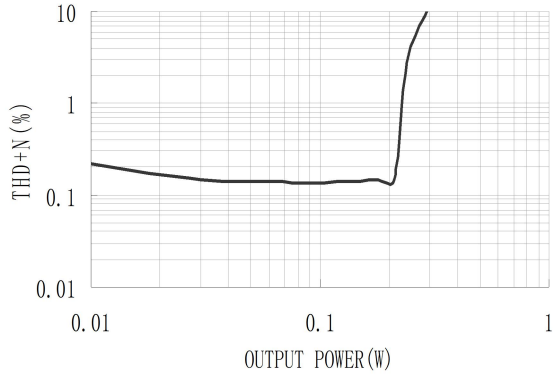


THD+N vs OutputPower VDD=2.5V, RL=8Ω, and f=1KHz

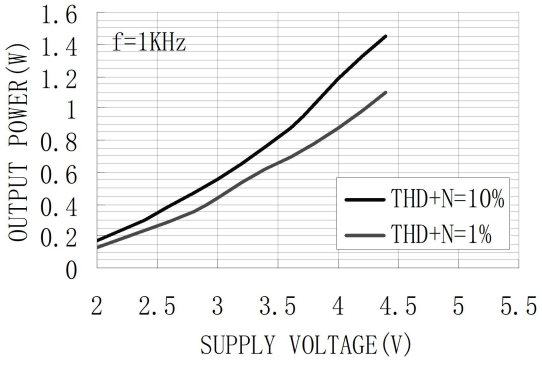
THD+N vs OutputPower VDD=3.3V, RL=4Ω, and f=1KHz

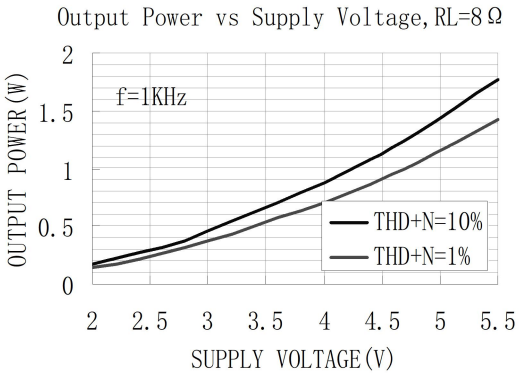


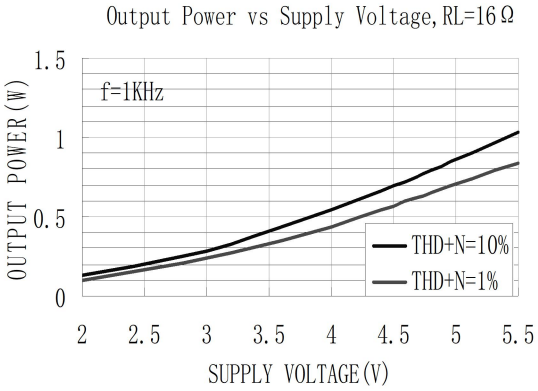
THD+N vs OutputPower VDD=2.5V, RL=4Ω, and f=1KHz



Output Power vs Supply Voltage, RL=4Ω



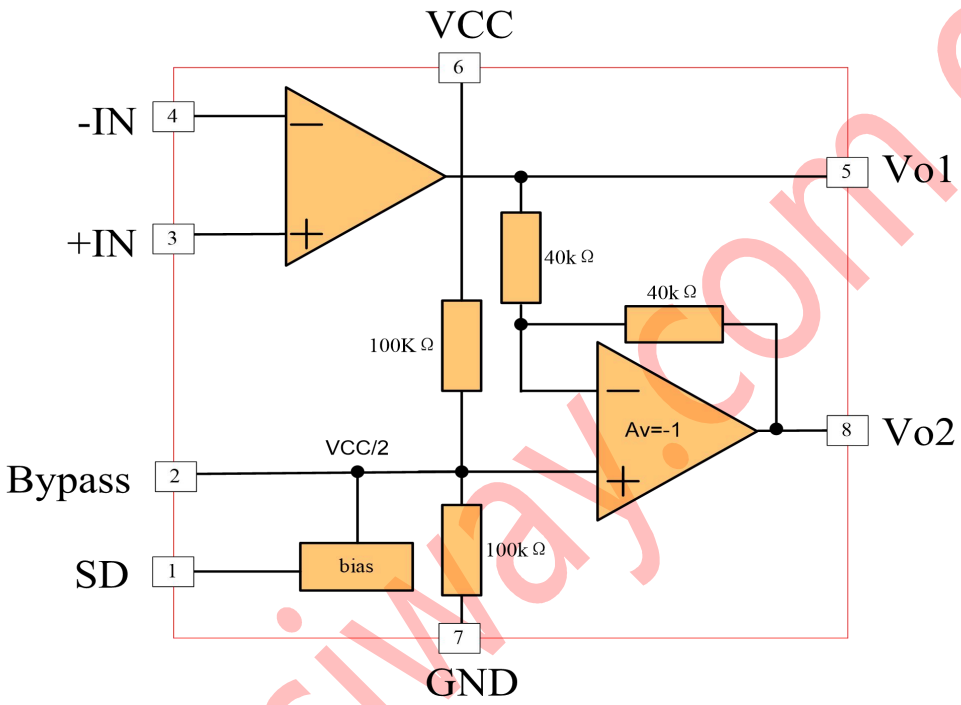




10application note

10.1Chip basic structure description

NS8002It is an audio power amplifier with double-ended output. It integrates two operational amplifiers. The gain of the first amplifier can be set by adjusting the feedback resistor, and the latter is an inverting follower of the voltage, thus forming an amplified drive circuit with a differential output whose gain can be configured. Its principle block diagram is:



10.2Chip digital logic characteristics

surface1Shutdown Signal Digital Logic Characteristics

parameter	minimum value	typical value	maximum value	unit	illustrate
The supply voltage is5V					
VIH		1.5		V	
VIL		1.3		V	
The supply voltage is3V					
VIH		1.3		V	
VIL		1.0		V	

10.3External Resistor Configuration

As shown in the application diagram, the gain of the op amp is controlled by an external resistorR_f,$R_i$decided, its gain isA_v=2xR_f/R_i, the chip passesV_{O1},V_{O2}Output to load, bridge connection.

The bridge connection method has several advantages over single-ended output: First, it saves the external DC blocking filter capacitor. For single-ended output, if the DC blocking capacitor is not connected, there will be a DC voltage at the output terminal, resulting in a DC current output after power-on, which will waste power consumption and easily damage the audio. The second is that the double-ended output is actually a push-pull output. Under the same output voltage, the driving power is increased to single-ended4times, the power output is large.

10.4External Capacitor Configuration

Excessive input capacitance increases cost and area, which is very unfavorable for applications with tight cost and area. Obviously, it is important to determine how much capacitance to use to accomplish the coupling. In fact, in many applications, speakers (Speaker) are not able to reproduce below100Hz- 150Hzlow-frequency sounds. Input coupling capacitance*Ci*(and*Ri*Forming a first-order high-pass) determines the low-frequency response, and the calculation formula is:

$$fc- \frac{1}{2-*Ri*Ci}$$

Therefore, using a large capacitor does not improve the performance of the system. In addition to considering the performance of the system, the suppression performance of switching/switching noise is affected by the capacitance. If the coupling capacitance is large, the delay of the feedback network will be large, resulting inpopNoise occurs, so a small coupling capacitor can reduce this noise.

10.5Chip power consumption

Power consumption is one of the key indicators for the amplifier. The maximum self-power consumption of the differential output amplifier is:

$$P_{dmax}- 4* \frac{VDD_2}{2-_2*R_L}$$

It must be noted that self power dissipation is a function of output power. When designing the circuit, it is not possible to make the junction temperature inside the chip higher than the normal operating temperature. According to the thermal resistance of the chip-$_{JA}$To design, you can increase the heat dissipation performance by dissipating copper and platinum yourself. If the chip still does not meet the requirements, you need to increase the load resistance, reduce the power supply voltage or lower the ambient temperature to solve it.

10.6 Power Bypass

In the application of the amplifier, the bypass design of the power supply is very important, especially for the noise performance and power supply voltage suppression performance of the application scheme. In the design, the bypass capacitor should be as close as possible to the chip and the power supply pin. Typical capacitance is10uFof electrolytic capacitors and on0.1uFof ceramic capacitors.

existNS8002application circuit, another capacitorC_B(catchBYPpins) are also very critical, affecting thePSRR, Switching/switching noise performance. general option0.1uF~1uFof ceramic capacitors.

10.7power down mode

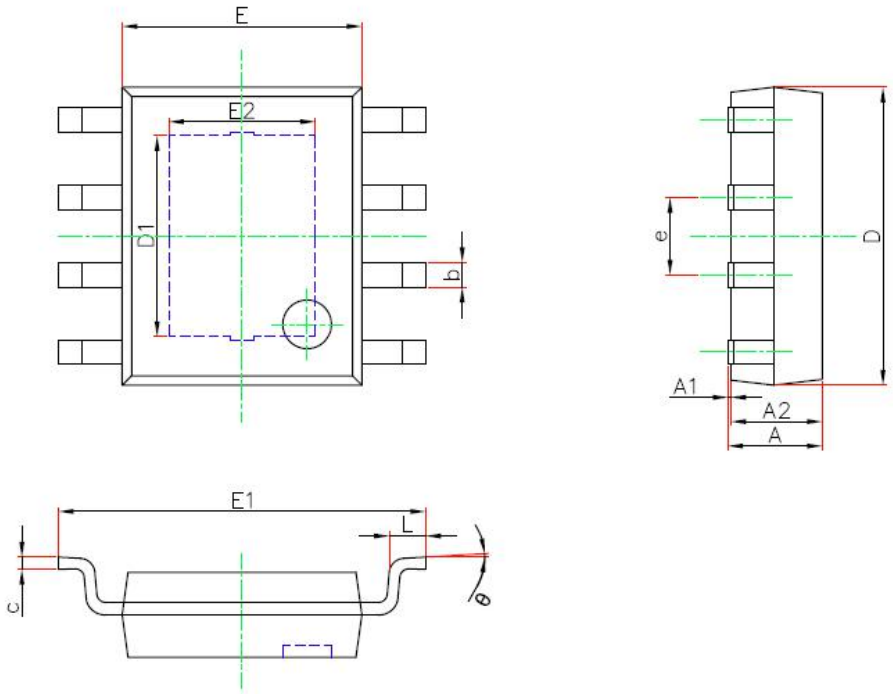
In order to save power, the amplifier can be turned off when not in use,NS8002There is a power-down control pin, which can control whether the amplifier works. The level of the control pin must be connected to the control signal that meets the interface requirements, otherwise the chip may enter an indeterminate state and cannot enter the power-down mode, and its self-power consumption is not reduced, and the purpose of power saving cannot be achieved.

11Version modification history

Disclaimer: Shenzhen Nationway Technology Co., Ltd. reserves the right to modify product information and product specifications at any time without notice. The right to interpret this manual belongs to Shenzhen Nationway Technology Co., Ltd. and is responsible for the final interpretation .

12Package information

ESOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°